Grant agreement for: Collaborative project*

Annex I - "Description of Work"

Project acronym: NAVOLCHI

Project full title: " Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection "

Grant agreement no: 288869

Date of last change: 2011-06-03

Preparation of the DoW date:

Table of Contents

Part A

Workplan Tables

A1:
Project summary

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

One form per project

General information

Project title [3]	Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection		
Starting date [4]			
Duration in months [5]	36		
Call (part) identifier [6]	FP7-ICT-2011-7		
Activity code(s) most relevant to your topic [7]	:		
Free keywords [8]	Silicon-on-Insulator, Optical Interconnect, Plasmonic Devices		

Abstract [9]

The NAVOLCHI project explores, develops and demonstrates a novel nano-scale plasmonic chip-to-chip and system-in-package interconnection platform to overcome the bandwidth, foot-print and power consumption limitations of todays electrical and optical interconnect solutions. The technology exploits the ultra-compact dimensions and fast electronic interaction times offered by surface plasmon polaritons to build plasmonic transceivers with a few square-micron footprints and speeds only limited by the RC constants. Key elements developed in this project are monolithically integrated plasmonic lasers, modulators, amplifiers and detectors on a CMOS platform. The transceivers will be interconnected by free space and fiber connect schemes. The plasmonic transceiver concept aims at overcoming the challenges posed by the need for massive parallel interchip communications. Yet, it is more fundamental as the availability of cheap miniturized transmitters and detectors on a single chip will enable new applications in sensing, biomedical testing and many other fields where masses of lasers and detectors are need to e.g. analyze samples. Economically, the suggested technology is a viable approach for a massive monolithic integration of optoelectronic functions on Si substrates as it relies to the most part on the standardized processes offered by the silicon industry. In addition, the design and production cost of plasmonic devices are extremely low and with the dimension 100 times smaller over conventional devices they will require much lower energy to transfer data over short ranges of multi-processor cluster systems. The project is disruptive and challenging but it is clearly within the area of expertise of the consortium. It actually builds on the partners prior art such as demonstration of the first nano-scale plasmonic pillar laser. This project has the potential to create novel high-impact technologies by taking advantage of the manifold possibilities offered by plasmonic effects.

A2:
List of Beneficiaries

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

List of Beneficiaries

No	Name	Short name	Country	Project entry month[10]	Project exit month
1	Karlsruher Institut fuer Technologie	KIT	Germany	1	36
2	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMCV	Belgium	1	36
3	TECHNISCHE UNIVERSITEIT EINDHOVEN	TU/e	Netherlands	1	36
4	RESEARCH AND EDUCATION LABORATORY IN INFORMATION TECHNOLOGIES	AIT	Greece	1	36
5	UNIVERSITAT DE VALENCIA	UVEG	Spain	1	36
6	STMICROELECTRONICS SRL	ST	Italy	1	36
7	UNIVERSITEIT GENT	Ugent	Belgium	1	36

A3:
Budget Breakdown

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

One Form per Project

Participant number in this project [11]	Participant short name	Fund. % [12]	Ind. costs [13]	Estimated eligible costs (whole duration of the project)					Requested EU contribution
				RTD / Innovation (A)	Demonstration (B)	Management (C)	Other (D)	Total A+B+C+D	
1	KIT	75.0	T	484,074.00	0.00	132,560.00	0.00	616,634.00	495,615.00
2	IMCV	75.0	A	508,818.00	0.00	4,400.00	0.00	513,218.00	386,013.00
3	TU/e	75.0	A	462,120.00	0.00	15,634.00	0.00	477,754.00	362,224.00
4	AIT	75.0	A	386,251.00	0.00	15,300.00	0.00	401,551.00	304,988.00
5	UVEG	75.0	T	395,760.00	0.00	14,720.00	0.00	410,480.00	311,540.00
6	ST	50.0	A	781,880.00	0.00	21,360.00	0.00	803,240.00	411,700.00
7	Ugent	75.0	T	170,560.00	0.00	0.00	0.00	170,560.00	127,920.00
Total				3,189,463.00	0.00	203,974.00	0.00	3,393,437.00	2,400,000.00

Note that the budget mentioned in this table is the total budget requested by the Beneficiary and associated Third Parties.

*** The following funding schemes are distinguished**

Collaborative Project (if a distinction is made in the call please state which type of Collaborative project is referred to: (i) Small of medium-scale focused research project, (ii) Large-scale integrating project, (iii) Project targeted to special groups such as SMEs and other smaller actors), Network of Excellence, Coordination Action, Support Action.

1. Project number

The project number has been assigned by the Commission as the unique identifier for your project, and it cannot be changed. The project number **should appear on each page of the grant agreement preparation documents** to prevent errors during its handling.

2. Project acronym

Use the project acronym as indicated in the submitted proposal. It cannot be changed, unless agreed during the negotiations. The same acronym **should appear on each page of the grant agreement preparation documents** to prevent errors during its handling.

3. Project title

Use the title (preferably no longer than 200 characters) as indicated in the submitted proposal. Minor corrections are possible if agreed during the preparation of the grant agreement.

4. Starting date

Unless a specific (fixed) starting date is duly justified and agreed upon during the preparation of the Grant Agreement, the project will start on the first day of the month following the entry info force of the Grant Agreement (NB : entry into force = signature by the Commission). Please note that if a fixed starting date is used, you will be required to provide a detailed justification on a separate note.

5. Duration

Insert the duration of the project in full months.

6. Call (part) identifier

The Call (part) identifier is the reference number given in the call or part of the call you were addressing, as indicated in the publication of the call in the Official Journal of the European Union. You have to use the identifier given by the Commission in the letter inviting to prepare the grant agreement.

7. Activity code

Select the activity code from the drop-down menu.

8. Free keywords

Use the free keywords from your original proposal; changes and additions are possible.

9. Abstract

10. The month at which the participant joined the consortium, month 1 marking the start date of the project, and all other start dates being relative to this start date.

11. The number allocated by the Consortium to the participant for this project.

12. Include the funding % for RTD/Innovation – either 50% or 75%

13. Indirect cost model

A: Actual Costs
S: Actual Costs Simplified Method
T: Transitional Flat rate
F :Flat Rate

Workplan Tables

Project number

288869

Project title

NAVOLCHI—Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Call (part) identifier

FP7-ICT-2011-7

Funding scheme

Collaborative project

WT1
List of work packages

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

LIST OF WORK PACKAGES (WP)

WP Number [53]	WP Title	Type of activity [54]	Lead beneficiary number [55]	Person-months [56]	Start month [57]	End month [58]
WP 1	Project Management	MGT	1	24.00	1	36
WP 2	Definition and specifications of plasmonic chip-to-chip interconnection platform	RTD	4	41.00	1	36
WP 3	Plasmonic transmitter	RTD	3	59.00	1	30
WP 4	Plasmonic receiver	RTD	5	80.00	1	36
WP 5	Optical and electrical interfaces for plasmonic interconnection platform	RTD	2	60.00	1	36
WP 6	Integration, characterization and testing	RTD	6	44.00	1	36
WP 7	Exploitation and Dissemination	RTD	4	24.00	1	36
			Total	332.00		

WT2:
List of Deliverables

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

List of Deliverables - to be submitted for review to EC

Delive-rable Number [61]	Deliverable Title	WP number [53]	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D1.1	Project web site with .eu domain (M 01) and continuous update	1	1	4.00	O	PU	1
D1.2	Project reference online manual.	1	1	2.00	O	RE	3
D1.3	Project quality online assurance manual:	1	1	2.00	O	RE	6
D1.4	Intermediate Progress Report	1	1	2.00	R	PU	9
D1.5	Intermediate Progress Report	1	1	2.00	R	RE	27
D2.1	Definition of chip-to-chip interconnection system environment and specification	2	6	7.00	R	RE	3
D2.2	Definition of plasmonic devices	2	4	7.00	R	RE	12
D2.3	Investigation of chip-to-chip interconnection-level specifications employing new plasmonic devices	2	4	6.75	R	RE	24
D2.4	Interface and plasmonic interconnect models and reports	2	6	4.00	R	RE	24
D2.5	Techno-economical evaluation with respect to the cost efficiency and green aspects	2	4	14.25	R	PU	30

WT2:
List of Deliverables

Delive-rable Number [61]	Deliverable Title	WP number [53]	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D2.6	Report on new applications and their opportunities	2	4	2.00	R	PU	36
D3.1	Report on studies of optimized structure for metallic/ plasmonic nano-laser and its coupling to Si WG	3	3	6.25	R	CO	12
D3.2	Report on modelling of the modulator structure	3	1	6.25	R	CO	12
D3.3	Fabrication of of plasmonic laser device	3	3	25.25	R	CO	24
D3.4	Report on fabrication of modulators	3	1	21.25	R	CO	24
D4.1	Designs of plasmonic amplifiers	4	4	11.20	R	CO	18
D4.2	Report on optical properties of QDs layers and polymer nanocomposites	4	4	27.20	R	PU	18
D4.3	Designs of plasmonic photodetectors	4	4	8.20	R	CO	24
D4.4	Report on SPP amplifiers by using QDs	4	2	14.20	R	PU	30
D4.5	Report on Plasmonic photodetectors	4	5	19.20	R	PU	33
D5.1	DDCM specification document	5	6	10.00	R	CO	6
D5.2	DDCM with electrical PHY design and	5	6	10.00	R	CO	12

WT2:
List of Deliverables

Delive-rable Number [61]	Deliverable Title	WP number [53]	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
	verification data base						
D5.3	Compact optical filters (2nm bandwidth, >30nm FSR) and first generation beam shapers	5	2	9.00	R	CO	21
D5.4	Generic DDCM compatible with plasmonic-based PHY specification document	5	6	9.00	R	PU	24
D5.5	Report on plasmonic waveguide couplers	5	2	14.00	R	CO	24
D5.6	Generic DDCM compatible with plasmonic-based PHY design and verification data base	5	6	3.00	R	CO	30
D5.7	Second generation beam shapers (distance 1mm, with bandwidth > 10nm and efficiency > 3dB)	5	2	5.00	P	CO	33
D6.1	Report on characterization results of all plasmonic devices	6	3	10.00	R	RE	27
D6.2	Report on characterization results of all optical interface plasmonic passive components	6	1	4.00	R	RE	27
D6.3	Report on chip to chip interconnect characterization	6	6	20.00	R	PU	36

WT2:
List of Deliverables

Delive-rable Number [61]	Deliverable Title	WP number [53]	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D6.4	Report on plasmonic chip-to-chip interconnect prototype testing and evaluation	6	4	10.00	R	PU	36
D7.1	First report on NAVOLCHI dissemination and promotion activities	7	6	2.00	R	RE	18
D7.2	First report on NAVOLCHI exploitation activities	7	4	2.00	R	RE	18
D7.3	Mirror Deliverable of D7.1, which will be available to the public on the website.	7	3	4.00	R	PU	18
D7.4	Intermediate report on recent achievements.	7	4	2.00	R	PU	18
D7.5	Reports on the impact and outcome of the organized promotion events.	7	4	4.00	R	PU	36
D7.6	Final report on NAVOLCHI dissemination and promotion activities	7	4	4.00	R	RE	36
D7.7	Dissemination kit	7	4	6.00	O	PU	36
			Total	320.00			

WT3:
Work package description

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

One form per Work Package

Work package number [53]	WP1	Type of activity [54]	MGT
Work package title	Project Management		
Start month	1		
End month	36		
Lead beneficiary number [55]	1		

Objectives

Description of work and role of partners

Person-Months per Participant

Participant number [10]	Participant short name [11]	Person-months per participant
1	KIT	16.00
2	IMCV	1.00
3	TU/e	1.00
4	AIT	2.00
5	UVEG	2.00
6	ST	2.00
	Total	24.00

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D1.1	Project web site with .eu domain (M 01) and continuous update	1	4.00	O	PU	1
D1.2	Project reference online manual.	1	2.00	O	RE	3
D1.3	Project quality online assurance manual:	1	2.00	O	RE	6
D1.4	Intermediate Progress Report	1	2.00	R	PU	9
D1.5	Intermediate Progress Report	1	2.00	R	RE	27
		Total	12.00			

Description of deliverables

WT3:
Work package description

D1.1) Project web site with .eu domain (M 01) and continuous update: Project web site with .eu domain (M1) and continuous update. _Short project fact sheet (≈2 pages) and short project presentation (few slides, mostly graphical, for Commission use and project web site)_ [month 1]

D1.2) Project reference online manual.: Project reference online manual. This document will incorporate all procedures concerning the technical and administrative management of the project. [month 3]

D1.3) Project quality online assurance manual:: Project quality online assurance manual: This document will set the procedures to achieve deliverables and deliveries of adequate quality [month 6]

D1.4) Intermediate Progress Report: Intermediate Progress Report (IPR) [month 9]

D1.5) Intermediate Progress Report: Intermediate Progress Report (IPR) [month 27]

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead benefi-ciary number	Delivery date from Annex I [60]	Comments

WT3:
Work package description

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

One form per Work Package

Work package number [53]	WP2	Type of activity [54]	RTD
Work package title	Definition and specifications of plasmonic chip-to-chip interconnection platform		
Start month	1		
End month	36		
Lead beneficiary number [55]	4		

Objectives

Description of work and role of partners

Person-Months per Participant

Participant number [10]	Participant short name [11]	Person-months per participant
1	KIT	2.00
2	IMCV	1.00
3	TU/e	6.00
4	AIT	18.00
5	UVEG	2.00
6	ST	12.00
	Total	41.00

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D2.1	Definition of chip-to-chip interconnection system environment and specification	6	7.00	R	RE	3
D2.2	Definition of plasmonic devices	4	7.00	R	RE	12
D2.3	Investigation of chip-to-chip interconnection-level specifications employing new plasmonic devices	4	6.75	R	RE	24
D2.4	Interface and plasmonic interconnect models and reports	6	4.00	R	RE	24
D2.5	Techno-economical evaluation with respect to the cost efficiency and green aspects	4	14.25	R	PU	30

WT3:
Work package description

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D2.6	Report on new applications and their opportunities	4	2.00	R	PU	36
		Total	41.00			

Description of deliverables

D2.1) Definition of chip-to-chip interconnection system environment and specification: [month 3]

D2.2) Definition of plasmonic devices: Definition of plasmonic devices, requirements and specification of chip-to-chip interconnection system environment. Initial plasmonic device design requirement and specifications are issued [month 12]

D2.3) Investigation of chip-to-chip interconnection-level specifications employing new plasmonic devices: Investigation of chip-to-chip interconnection-level specifications employing new plasmonic devices [month 24]

D2.4) Interface and plasmonic interconnect models and reports: Interface and plasmonic interconnect models and reports [month 24]

D2.5) Techno-economical evaluation with respect to the cost efficiency and green aspects: Techno-economical evaluation with respect to the cost efficiency and green aspects [month 30]

D2.6) Report on new applications and their opportunities: Report on new applications and their opportunities [month 36]

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead benefi-ciary number	Delivery date from Annex I [60]	Comments
MS1	Definition of chip-to-chip interconnection system environment and specification	4	3	
MS2	Definition of plasmonic devices and material properties for chip-to-chip interconnection	4	6	
MS3	Development of a system and device simulation platform.	4	18	
MS4	Definition Derivation of the interconnection level specification employing developed plasmonic photo	6	18	
MS5	Digital domain to plasmonic domain interface specification and VHDL modelling	6	21	
MS6	Plasmonic interconnect VHDL modelling	6	24	
MS7	Investigation of the cost and power consumption efficiency of the developed plasmonic devices and in	4	28	

WT3:
Work package description

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

One form per Work Package

Work package number [53]	WP3	Type of activity [54]	RTD
Work package title	Plasmonic transmitter		
Start month	1		
End month	30		
Lead beneficiary number [55]	3		

Objectives

Description of work and role of partners

Person-Months per Participant

Participant number [10]	Participant short name [11]	Person-months per participant
1	KIT	26.00
2	IMCV	3.00
3	TU/e	29.00
6	ST	1.00
	Total	59.00

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D3.1	Report on studies of optimized structure for metallic/plasmonic nano-laser and its coupling to Si WG	3	6.25	R	CO	12
D3.2	Report on modelling of the modulator structure	1	6.25	R	CO	12
D3.3	Fabrication of of plasmonic laser device	3	25.25	R	CO	24
D3.4	Report on fabrication of modulators	1	21.25	R	CO	24
		Total	59.00			

Description of deliverables

D3.1) Report on studies of optimized structure for metallic/plasmonic nano-laser and its coupling to Si WG: Report on studies of optimized structure for metallic/plasmonic nano-laser and its coupling to Si WG [month 12]

D3.2) Report on modelling of the modulator structure: Report on modelling of the modulator structure [month 12]

D3.3) Fabrication of of plasmonic laser device: Fabrication of of plasmonic laser device [month 24]

D3.4) Report on fabrication of modulators: Report on fabrication of modulators [month 24]

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead beneficiary number	Delivery date from Annex I [60]	Comments
MS8	Decision on an optimized structure for metallic/plasmonic nano-laser and its coupling to Si waveguid	3	6	We will aim for a structure that will in theory give between 15 and 40% quantum efficiency, when measuring the amount of light coupled into the Si waveguide
MS9	Decision on a optimized structure for plasmonic modulator	1	6	Length of 20 um and with an extionction ratio of at least 1dB
MS10	Grown wafer structure for plasmonic lasers	2	12	
MS11	Fabrication of plasmonic modulator on a SOI platform	1	15	
MS12	Decision on a optimized structure for plasmonic modulator with a maximum loss of 20dB	1	18	
MS13	Initial characterization of unbonded plasmonic lasers	3	18	We will aim to have achieve lasers with thresholds below 1mA, and likely below 500 micro amps
MS14	Initial testing and characterization of plasmonic modulators	1	21	Modulators with 20 um length and 2V peak-to-peak voltage swing
MS15	Initial testing of bonded plasmonic lasers	3	24	We will aim to have achieve at least 100 □W power coupled into the Si waveguide.

WT3:
Work package description

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

One form per Work Package

Work package number [53]	WP4	Type of activity [54]	RTD
Work package title	Plasmonic receiver		
Start month	1		
End month	36		
Lead beneficiary number [55]	5		

Objectives

Description of work and role of partners

Person-Months per Participant

Participant number [10]	Participant short name [11]	Person-months per participant
1	KIT	3.00
2	IMCV	11.00
4	AIT	9.00
5	UVEG	32.00
6	ST	1.00
7	Ugent	24.00
	Total	80.00

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D4.1	Designs of plasmonic amplifiers	4	11.20	R	CO	18
D4.2	Report on optical properties of QDs layers and polymer nanocomposites	4	27.20	R	PU	18
D4.3	Designs of plasmonic photodetectors	4	8.20	R	CO	24
D4.4	Report on SPP amplifiers by using QDs	2	14.20	R	PU	30
D4.5	Report on Plasmonic photodetectors	5	19.20	R	PU	33
		Total	80.00			

Description of deliverables

D4.1) Designs of plasmonic amplifiers: Designs of plasmonic amplifiers [month 18]

D4.2) Report on optical properties of QDs layers and polymer nanocomposites: Report on optical properties of QDs layers and polymer nanocomposites [month 18]

D4.3) Designs of plasmonic photodetectors: Designs of plasmonic photodetectors [month 24]

D4.4) Report on SPP amplifiers by using QDs: Report on SPP amplifiers by using QDs [month 30]

D4.5) Report on Plasmonic photodetectors: Report on Plasmonic photodetectors [month 33]

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead beneficiary number	Delivery date from Annex I [60]	Comments
MS16	Demonstration of decision on optimized structures for plasmonic amplifiers	5	12	Amplifiers with 10dB gain, 30nm bandwith
MS17	Synthesis of nanoparticles with gain at 1550nm	7	12	
MS18	Demonstration of conductive QD layers with photoconductive properties	5	15	
MS19	Demonstration of metal-(lithographic) polymer and QD metal-(lithographic) polymer nanocompo-sites	5	15	Demonstration of metal-(lithographic) polymer and QD metal-(lithographic) polymer nanocompo-sites with response to telecom photons
MS20	Demonstration and decision on photodetector operation: nano-gap (MIM) vs Schottky/heterostructure	5	18	
MS21	Electroluminscence from QD stack embedded within conductive oxides (>1uW)	2	18	
MS22	Demonstration of plasmonic amplifiers with optical pumping exhibiting 10dB gain	2	21	
MS23	Operation of QD based photodetector with responsivity > 0.1A/W	5	24	
MS24	Demonstration of SPP amplifiers with electrical injection exhibiting 10dB/cm gain	5	30	

WT3:
Work package description

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

One form per Work Package

Work package number [53]	WP5	Type of activity [54]	RTD
Work package title	Optical and electrical interfaces for plasmonic interconnection platform		
Start month	1		
End month	36		
Lead beneficiary number [55]	2		

Objectives

Description of work and role of partners

Person-Months per Participant

Participant number [10]	Participant short name [11]	Person-months per participant
1	KIT	12.00
2	IMCV	14.00
5	UVEG	4.00
6	ST	30.00
	Total	60.00

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D5.1	DDCM specification document	6	10.00	R	CO	6
D5.2	DDCM with electrical PHY design and verification data base	6	10.00	R	CO	12
D5.3	Compact optical filters (2nm bandwidth, >30nm FSR) and first generation beam shapers	2	9.00	R	CO	21
D5.4	Generic DDCM compatible with plasmonic-based PHY specification document	6	9.00	R	PU	24
D5.5	Report on plasmonic waveguide couplers	2	14.00	R	CO	24
D5.6	Generic DDCM compatible with plasmonic-based PHY design and verification data base	6	3.00	R	CO	30

WT3:
Work package description

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D5.7	Second generation beam shapers (distance 1mm, with bandwidth > 10nm and efficiency > 3dB)	2	5.00	P	CO	33
		Total	60.00			

Description of deliverables

D5.1) DDCM specification document: DDCM specification document [month 6]

D5.2) DDCM with electrical PHY design and verification data base: DDCM with electrical PHY design and verification data base [month 12]

D5.3) Compact optical filters (2nm bandwidth, >30nm FSR) and first generation beam shapers: Compact optical filters (2nm bandwidth, >30nm FSR) and first generation beam shapers [month 21]

D5.4) Generic DDCM compatible with plasmonic-based PHY specification document: Generic DDCM compatible with plasmonic-based PHY specification document [month 24]

D5.5) Report on plasmonic waveguide couplers: Report on plasmonic waveguide couplers [month 24]

D5.6) Generic DDCM compatible with plasmonic-based PHY design and verification data base: Generic DDCM compatible with plasmonic-based PHY design and verification data base [month 30]

D5.7) Second generation beam shapers (distance 1mm, with bandwidth > 10nm and efficiency > 3dB): Second generation beam shapers (distance 1mm, with bandwidth > 10nm and efficiency > 3dB) [month 33]

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead benefi-ciary number	Delivery date from Annex I [60]	Comments
MS25	Decision on optimized plasmonic waveguide couplers	1	6	
MS26	Fabrication of plasmonic waveguide couplers with less than 3 dB coupling loss	1	12	
MS27	Design of first generation beam shapers and compact optical filters	2	12	Design of first generation beam shapers (5dB loss, 100um distance) and compact optical filters (3nm bandwidth, 10dB suppression, 30nm free spectral range)(
MS28	DDCM with electrical PHY design and verification	6	12	
MS29	Data codecs for power consumption reduction	6	15	
MS30	Decision on plasmonic waveguide couplers with less than 3 dB coupling loss	1	15	

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead beneficiary number	Delivery date from Annex I [60]	Comments
MS31	Fabrication of compact optical filters and first generation beam shapers	2	18	
MS32	Data codecs for error detection and correction	6	18	
MS33	Design of second generationbeam shapers	2	24	Design of second generationbeam shapers (3dB loss, 1mm distance)
MS34	Generic DDCM compatible with plasmonic-based PHY	6	24	
MS35	Fabrication of compact optical filters and first generation beam shapers	2	30	Fabrication of compact optical filters (3nm bandwidth, 10dB suppression, 30nm free spectral range) and first generation beam shapers (5dB loss, 100um distance)
MS36	DDCM evolution for NiP solutions	6	30	

WT3:
Work package description

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

One form per Work Package

Work package number [53]	WP6	Type of activity [54]	RTD
Work package title	Integration, characterization and testing		
Start month	1		
End month	36		
Lead beneficiary number [55]	6		

Objectives

Description of work and role of partners

Person-Months per Participant

Participant number [10]	Participant short name [11]	Person-months per participant
1	KIT	4.00
2	IMCV	3.00
3	TU/e	3.00
4	AIT	10.00
5	UVEG	2.00
6	ST	22.00
	Total	44.00

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D6.1	Report on characterization results of all plasmonic devices	3	10.00	R	RE	27
D6.2	Report on characterization results of all optical interface plasmonic passive components	1	4.00	R	RE	27
D6.3	Report on chip to chip interconnect characterization	6	20.00	R	PU	36
D6.4	Report on plasmonic chip-to-chip interconnect prototype testing and evaluation	4	10.00	R	PU	36
		Total	44.00			

Description of deliverables

WT3:
Work package description

D6.1) Report on characterization results of all plasmonic devices: Report on characterization results of all plasmonic devices [month 27]

D6.2) Report on characterization results of all optical interface plasmonic passive components: Report on characterization results of all optical interface plasmonic passive components [month 27]

D6.3) Report on chip to chip interconnect characterization: Report on chip to chip interconnect characterization [month 36]

D6.4) Report on plasmonic chip-to-chip interconnect prototype testing and evaluation: Report on plasmonic chip-to-chip interconnect prototype testing and evaluation [month 36]

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead benefi-ciary number	Delivery date from Annex I [60]	Comments
MS37	Plasmonic active device characterization results	1	12	
MS38	Plasmonic passive components characterization results with a 1dB coupling loss	1	24	
MS39	Concept for system integration developed	4	27	
MS40	Individual plasmonic devices characterization, testing and evaluation	3	30	
MS41	Chip to chip interconnect characterization	6	33	
MS42	Plasmonic components integration to demonstrate chip-to-chip interconnect	4	33	
MS43	Plasmonic chip to chip interconnect prototype testing and evaluation	6	36	

WT3:
Work package description

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

One form per Work Package

Work package number [53]	WP7	Type of activity [54]	RTD
Work package title	Exploitation and Dissemination		
Start month	1		
End month	36		
Lead beneficiary number [55]	4		

Objectives

Description of work and role of partners

Person-Months per Participant

Participant number [10]	Participant short name [11]	Person-months per participant
1	KIT	3.00
2	IMCV	1.00
3	TU/e	1.00
4	AIT	8.00
5	UVEG	1.00
6	ST	10.00
	Total	24.00

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D7.1	First report on NAVOLCHI dissemination and promotion activities	6	2.00	R	RE	18
D7.2	First report on NAVOLCHI exploitation activities	4	2.00	R	RE	18
D7.3	Mirror Deliverable of D7.1, which will be available to the public on the website.	3	4.00	R	PU	18
D7.4	Intermediate report on recent achievements.	4	2.00	R	PU	18
D7.5	Reports on the impact and outcome of the organized promotion events.	4	4.00	R	PU	36

WT3:
Work package description

List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D7.6	Final report on NAVOLCHI dissemination and promotion activities	4	4.00	R	RE	36
D7.7	Dissemination kit	4	6.00	O	PU	36
		Total	24.00			

Description of deliverables

D7.1) First report on NAVOLCHI dissemination and promotion activities: First report on NAVOLCHI dissemination and promotion activities. The "Report on dissemination and promotion of the project results" will include a sum-mary table according to the template provided by the Commission, and explain further details as appropriate. [month 18]

D7.2) First report on NAVOLCHI exploitation activities: First report on NAVOLCHI exploitation plans. [month 18]

D7.3) Mirror Deliverable of D7.1, which will be available to the public on the website.: Mirror Deliverable of D7.1 which will be available to the public on the website. This report will be a filtered version of D7.1 and might be extended in order to explain the activities to a broader audience. [month 18]

D7.4) Intermediate report on recent achievements.: Intermediate report on recent achievements. This report summarizes advances in the project for the general public. Precedence is given for publications in journals and on conferences. [month 18]

D7.5) Reports on the impact and outcome of the organized promotion events.: Report on the impact and outcomes of the organized promotion events. (Workshop, summer school, demonstration activities). [month 36]

D7.6) Final report on NAVOLCHI dissemination and promotion activities: Final report on NAVOLCHI dissemination and promotion activities. [month 36]

D7.7) Dissemination kit: The "dissemination kit" contains suitable material (e.g. texts and pictures including copyright clearance), which the Commission may use for its own dissemination of project results. These materials should become available also on the project web. [month 36]

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead benefi-ciary number	Delivery date from Annex I [60]	Comments
MS44	Dissemination of activities in the project's web site and continuous update	1	1	
MS45	Press release on start of project to the public distributed	4	2	
MS46	Identification of possible contributions to the industrial partners for commercialization	6	15	Identification of possible contributions to the industrial partners for commercialization and standardization.

WT3:
Work package description

Schedule of relevant Milestones

Milestone number [59]	Milestone name	Lead beneficiary number	Delivery date from Annex I [60]	Comments
MS47	Organization of workshop on silicon photonics interface for chip-to-chip communication	3	34	
MS48	Public web site for NAVOLCHI prepared to stay open for at least another year	1	36	
MS49	Press release distributed comprising key results with a public target audience	4	36	

WT4:
List of Milestones

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

List and Schedule of Milestones

Milestone number [59]	Milestone name	WP number [53]	Lead beneficiary number	Delivery date from Annex I [60]	Comments
MS1	Definition of chip-to-chip interconnection system environment and specification	WP2	4	3	
MS2	Definition of plasmonic devices and material properties for chip-to-chip interconnection	WP2	4	6	
MS3	Development of a system and device simulation platform.	WP2	4	18	
MS4	Definition Derivation of the interconnection level specification employing developed plasmonic photo	WP2	6	18	
MS5	Digital domain to plasmonic domain interface specification and VHDL modelling	WP2	6	21	
MS6	Plasmonic interconnect VHDL modelling	WP2	6	24	
MS7	Investigation of the cost and power consumption efficiency of the developed plasmonic devices and in	WP2	4	28	
MS8	Decision on an optimized structure for metallic/plasmonic nano-laser and its coupling to Si waveguid	WP3	3	6	We will aim for a structure that will in theory give between 15 and 40% quantum efficiency, when measuring the amount of light coupled into the Si waveguide
MS9	Decision on a optimized structure for plasmonic modulator	WP3	1	6	Length of 20 um and with an extionction ratio of at least 1dB

WT4:
List of Milestones

Milestone number [59]	Milestone name	WP number [53]	Lead beneficiary number	Delivery date from Annex I [60]	Comments
MS10	Grown wafer structure for plasmonic lasers	WP3	2	12	
MS11	Fabrication of plasmonic modulator on a SOI platform	WP3	1	15	
MS12	Decision on a optimized structure for plasmonic modulator with a maximum loss of 20dB	WP3	1	18	
MS13	Initial characterization of unbonded plasmonic lasers	WP3	3	18	We will aim to have achieve lasers with thresholds below 1mA, and likely below 500 micro amps
MS14	Initial testing and characterization of plasmonic modulators	WP3	1	21	Modulators with 20 um length and 2V peak-to-peak voltage swing
MS15	Initial testing of bonded plasmonic lasers	WP3	3	24	We will aim to have achieve at least 100 ☐W power coupled into the Si waveguide.
MS16	Demonstration of decision on optimized structures for plasmonic amplifiers	WP4	5	12	Amplifiers with 10dB gain, 30nm bandwith
MS17	Synthesis of nanoparticles with gain at 1550nm	WP4	7	12	
MS18	Demonstration of conductive QD layers with photoconductive properties	WP4	5	15	
MS19	Demonstration of metal-(lithographic) polymer and QD metal-(lithographic) polymer nanocompo-sites	WP4	5	15	Demonstration of metal-(lithographic) polymer and QD metal-(lithographic) polymer nanocompo-sites with response to telecom photons
MS20	Demonstration and decision on photodetector operation: nano-gap	WP4	5	18	

WT4:
List of Milestones

Milestone number [59]	Milestone name	WP number [53]	Lead beneficiary number	Delivery date from Annex I [60]	Comments
	(MIM) vs Schottky/ heterostructure				
MS21	Electroluminscence from QD stack embedded within conductive oxides (>1uW)	WP4	2	18	
MS22	Demonstration of plasmonic amplifiers with optical pumping exhibiting 10dB gain	WP4	2	21	
MS23	Operation of QD based photodetector with responsivity > 0.1A/W	WP4	5	24	
MS24	Demonstration of SPP amplifiers with electrical injection exhibiting 10dB/cm gain	WP4	5	30	
MS25	Decision on optimized plasmonic waveguide couplers	WP5	1	6	
MS26	Fabrication of plasmonic waveguide couplers with less than 3 dB coupling loss	WP5	1	12	
MS27	Design of first generation beam shapers and compact optical filters	WP5	2	12	Design of first generation beam shapers (5dB loss, 100um distance) and compact optical filters (3nm bandwidth, 10dB suppression, 30nm free spectral range)(
MS28	DDCM with electrical PHY design and verification	WP5	6	12	
MS29	Data codecs for power consumption reduction	WP5	6	15	
MS30	Decision on plasmonic waveguide couplers with less than 3 dB coupling loss	WP5	1	15	
MS31	Fabrication of compact optical filters and first	WP5	2	18	

WT4:
List of Milestones

Milestone number [59]	Milestone name	WP number [53]	Lead beneficiary number	Delivery date from Annex I [60]	Comments
	generation beam shapers				
MS32	Data codecs for error detection and correction	WP5	6	18	
MS33	Design of second generationbeam shapers	WP5	2	24	Design of second generationbeam shapers (3dB loss, 1mm distance)
MS34	Generic DDCM compatible with plasmonic-based PHY	WP5	6	24	
MS35	Fabrication of compact optical filters and first generation beam shapers	WP5	2	30	Fabrication of compact optical filters (3nm bandwidth, 10dB suppression, 30nm free spectral range) and first generation beam shapers (5dB loss, 100um distance)
MS36	DDCM evolution for NiP solutions	WP5	6	30	
MS37	Plasmonic active device characterization results	WP6	1	12	
MS38	Plasmonic passive components characterization results with a 1dB coupling loss	WP6	1	24	
MS39	Concept for system integration developed	WP6	4	27	
MS40	Individual plasmonic devices characterization, testing and evaluation	WP6	3	30	
MS41	Chip to chip interconnect characterization	WP6	6	33	
MS42	Plasmonic components integration to demonstrate chip-to-chip interconnect	WP6	4	33	

WT4:
List of Milestones

Milestone number [59]	Milestone name	WP number [53]	Lead beneficiary number	Delivery date from Annex I [60]	Comments
MS43	Plasmonic chip to chip interconnect prototype testing and evaluation	WP6	6	36	
MS44	Dissemination of activities in the project's web site and continuous update	WP7	1	1	
MS45	Press release on start of project to the public distributed	WP7	4	2	
MS46	Identification of possible contributions to the industrial partners for commercialization	WP7	6	15	Identification of possible contributions to the industrial partners for commercialization and standardization.
MS47	Organization of workshop on silicon photonics interface for chip-to-chip communication	WP7	3	34	
MS48	Public web site for NAVOLCHI prepared to stay open for at least another year	WP7	1	36	
MS49	Press release distributed comprising key results with a public target audience	WP7	4	36	

WT5:
Tentative schedule of Project Reviews

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

Tentative schedule of Project Reviews

Review number [65]	Tentative timing	Planned venue of review	Comments, if any

WT6:
Project Effort by Beneficiary and Work Package

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

Indicative efforts (man-months) per Beneficiary per Work Package

Beneficiary number and short-name	WP 1	WP 2	WP 3	WP 4	WP 5	WP 6	WP 7	Total per Beneficiary
1 - KIT	16.00	2.00	26.00	3.00	12.00	4.00	3.00	66.00
2 - IMCV	1.00	1.00	3.00	11.00	14.00	3.00	1.00	34.00
3 - TU/e	1.00	6.00	29.00	0.00	0.00	3.00	1.00	40.00
4 - AIT	2.00	18.00	0.00	9.00	0.00	10.00	8.00	47.00
5 - UVEG	2.00	2.00	0.00	32.00	4.00	2.00	1.00	43.00
6 - ST	2.00	12.00	1.00	1.00	30.00	22.00	10.00	78.00
7 - Ugent	0.00	0.00	0.00	24.00	0.00	0.00	0.00	24.00
Total	24.00	41.00	59.00	80.00	60.00	44.00	24.00	332.00

WT7:
Project Effort by Activity type per Beneficiary

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

Indicative efforts per Activity Type per Beneficiary

Activity type	Part. 1 KIT	Part. 2 IMCV	Part. 3 TU/e	Part. 4 AIT	Part. 5 UVEG	Part. 6 ST	Part. 7 Ugent	Total
1. RTD/Innovation activities								
WP 2	2.00	1.00	6.00	18.00	2.00	12.00	0.00	41.00
WP 3	26.00	3.00	29.00	0.00	0.00	1.00	0.00	59.00
WP 4	3.00	11.00	0.00	9.00	32.00	1.00	24.00	80.00
WP 5	12.00	14.00	0.00	0.00	4.00	30.00	0.00	60.00
WP 6	4.00	3.00	3.00	10.00	2.00	22.00	0.00	44.00
WP 7	3.00	1.00	1.00	8.00	1.00	10.00	0.00	24.00
Total Research	50.00	33.00	39.00	45.00	41.00	76.00	24.00	308.00
2. Demonstration activities								
Total Demo	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
3. Consortium Management activities								
WP 1	16.00	1.00	1.00	2.00	2.00	2.00	0.00	24.00
Total Management	16.00	1.00	1.00	2.00	2.00	2.00	0.00	24.00
4. Other activities								
Total other	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Total	66.00	34.00	40.00	47.00	43.00	78.00	24.00	332.00

WT8:
Project Effort and costs

Project Number [1]	288869	Project Acronym [2]	NAVOLCHI

Project efforts and costs

Benefi-ciary number	Beneficiary short name	Estimated eligible costs (whole duration of the project)						Requested EU contribution (€)
		Effort (PM)	Personnel costs (€)	Subcontracting (€)	Other Direct costs (€)	Indirect costs OR lump sum, flat-rate or scale-of-unit (€)	Total costs	
1	KIT	66.00	335,634.00	2,000.00	77,620.00	201,380.00	616,634.00	495,615.00
2	IMCV	34.00	229,059.00	4,400.00	25,350.00	254,409.00	513,218.00	386,013.00
3	TU/e	40.00	200,631.00	0.00	63,650.00	213,473.00	477,754.00	362,224.00
4	AIT	47.00	211,500.00	0.00	42,000.00	148,051.00	401,551.00	304,988.00
5	UVEG	43.00	176,550.00	40,000.00	55,000.00	138,930.00	410,480.00	311,540.00
6	ST	78.00	343,200.00	2,000.00	46,200.00	411,840.00	803,240.00	411,700.00
7	Ugent	24.00	80,000.00	0.00	26,600.00	63,960.00	170,560.00	127,920.00
	Total	332.00	1,576,574.00	48,400.00	336,420.00	1,432,043.00	3,393,437.00	2,400,000.00

1. Project number

The project number has been assigned by the Commission as the unique identifier for your project. It cannot be changed. The project number **should appear on each page of the grant agreement preparation documents (part A and part B)** to prevent errors during its handling.

2. Project acronym

Use the project acronym as given in the submitted proposal. It cannot be changed unless agreed so during the negotiations. The same acronym **should appear on each page of the grant agreement preparation documents (part A and part B)** to prevent errors during its handling.

53. Work Package number

Work package number: WP1, WP2, WP3, ..., WPn

54. Type of activity

For all FP7 projects each work package must relate to one (and only one) of the following possible types of activity (only if applicable for the chosen funding scheme – must correspond to the GPF Form Ax.v):

• **RTD/INNO =** Research and technological development including scientific coordination - applicable for Collaborative Projects and Networks of Excellence

• **DEM =** Demonstration - applicable for collaborative projects and Research for the Benefit of Specific Groups

• **MGT =** Management of the consortium - applicable for all funding schemes

• **OTHER =** Other specific activities, applicable for all funding schemes

• **COORD =** Coordination activities – applicable only for CAs

• **SUPP =** Support activities – applicable only for SAs

55. Lead beneficiary number

Number of the beneficiary leading the work in this work package.

56. Person-months per work package

The total number of person-months allocated to each work package.

57. Start month

Relative start date for the work in the specific work packages, month 1 marking the start date of the project, and all other start dates being relative to this start date.

58. End month

Relative end date, month 1 marking the start date of the project, and all end dates being relative to this start date.

59. Milestone number

Milestone number:MS1, MS2, …, MSn

60. Delivery date for Milestone

Month in which the milestone will be achieved. Month 1 marking the start date of the project, and all delivery dates being relative to this start date.

61. Deliverable number

Deliverable numbers in order of delivery dates: D1 – Dn

62. Nature

Please indicate the nature of the deliverable using one of the following codes

R = Report, **P** = Prototype, **D** = Demonstrator, **O** = Other

63. Dissemination level

Please indicate the dissemination level using one of the following codes:

• **PU =** Public

• **PP =** Restricted to other programme participants (including the Commission Services)

• **RE =** Restricted to a group specified by the consortium (including the Commission Services)

• **CO =** Confidential, only for members of the consortium (including the Commission Services)

• **Restreint UE =** Classified with the classification level "Restreint UE" according to Commission Decision 2001/844 and amendments

• **Confidentiel UE =** Classified with the mention of the classification level "Confidentiel UE" according to Commission Decision 2001/844 and amendments

• **Secret UE =** Classified with the mention of the classification level "Secret UE" according to Commission Decision 2001/844 and amendments

64. Delivery date for Deliverable

Month in which the deliverables will be available. Month 1 marking the start date of the project, and all delivery dates being relative to this start date

65. Review number

Review number: RV1, RV2, ..., RVn

66. Tentative timing of reviews

Month after which the review will take place. Month 1 marking the start date of the project, and all delivery dates being relative to this start date.

67. Person-months per Deliverable

The total number of person-month allocated to each deliverable.

PART B

COLLABORATIVE PROJECT

Table of Contents

B1. CONCEPT AND OBJECTIVES, PROGRESS BEYOND STATE-OF-THE-ART, S/T METHODOLOGY AND WORK PLAN

B1.1. Concept and project objective(s)

The goal of this project is to realize chip-to-chip and system-in-package chip to components interconnects with smallest footprint, power consumption at highest bit-rates by introducing novel plasmonic, CMOS compatible photonic technologies.

In order to obtain super fast processing capability, next generation processors will be realized with multi-core systems. Multicore systems have been identified as the most promising, scalable and power efficient method for integrating larger number of CMOS circuits. The transition to many-core microprocessor architectures is expected to drive increased chip-to-chip I/O bandwidth demands in processor, processor-memory interfaces and in multi-processor systems in the range of 200 Gbit/s to 1 Tbit/s [1]. To this point electrical interconnects are used. However, this technology not only suffers from limited bandwidths but also from electrical cross-talk, frequency-dependent loss (dispersion), and high power dissipation. Current photonic technologies, which are optimized for long distance telecommunication and data communication applications, do not meet the necessary metrics (footprint, power dissipation, form factor, cost, and signal integrity) needed for interconnects between high-speed electronic chips. Ideally, future generations of super high computing systems will rely on optical interconnects offering several terahertz bandwidths at low loss for on chip-to-chip and board-to-board communications with better crosstalk-noise immunity.

B1.1.1. *Concept of the Si-Plasmonic Chip-to-Chip and System-in-Package (SiP) Interconnection Platform*

Current systems are characterized by the following features, leading to design and manufacturing issues:

The ever decreasing feature size in CMOS silicon processes allows digital logic to shrink significantly between subsequent fabrication nodes, for example a shrink of 55% could be expected when comparing a digital IP implemented in 90nm and 65nm. However analogue and IO cells have been unable to match this rate of decrease, leading to increasingly pad limited designs in many complex SoCs. A pad-limited design can be viewed as wasteful since the digital logic is not implemented as densely as it was the only contributing factor to the device area.

The transition to sub 32nm design introduces a dichotomy between supporting low voltage, high speed IO logic; for example DDR3 1.5V @ 800MHz+; and higher voltage interconnect technologies as for example HDMI, SATA, USB3 etc. The lower voltage DDR3 interface requires a technology with gate

[1] I.A. Young, E. Mohammed, J.T.S. Liao, A.M. Kern, S. Palermo, B.A. Block, M.R. Reshotko, and P.L.D. Chang, "Optical I/O Technology for Tera-Scale Computing", IEEE J. of Solid State Circuits, Vol. 45, No. 1, pp. 235-248, January 2010.

oxide thickness of 30A, while HDMI would require a technology with 50A, which are incompatible requirements that can not be met within a standard process.

Splitting a traditional single System on Chip (SoC) into more dice in order to form a so called System-in-Package (SiP) allows to alleviate the aforementioned issues. An example SIP would comprise of a 32nm die comprising high speed CPUs, DDR3 controller(s) and differentiating IP, connected to a 55nm die comprising analogue PHYs. Thanks to the reduced set of analogue IP the 32nm die gets the maximum benefit from the shrink.

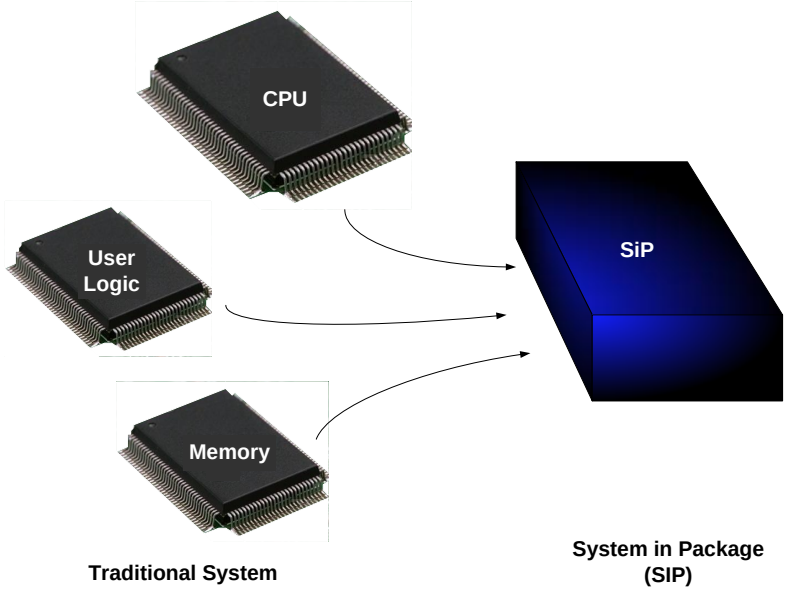

Figure 1.1.1 Example of heterogeneous integration of several dies into a System-in-Package (SiP)

Such a System in Package technology offers many significant benefits, including:

Footprint – More functionality fits into a small space. This extends Moore's Law and enables a new generation of tiny but powerful devices.

Speed – The average wire length becomes much shorter. Because propagation delay is proportional to the square of the wire length, overall performance increases.

Power – Keeping a signal on-chip reduces its power consumption by ten to a hundred times. Shorter wires also reduce power consumption by producing less parasitic capacitance. Reducing the power budget leads to less heat generation, extended battery life, and lower cost of operation.

Design – The vertical dimension adds a higher order of connectivity and opens a world of new design possibilities.

Heterogeneous integration – Circuit layers can be built with different processes, or even on different types of wafers. This means that components can be optimized to a much greater degree than if they were built together on a single wafer. Even more interesting, components with completely incompatible manufacturing could be combined in a single device (see Figure 1.1.1)

Circuit security - The stacked structure hinders attempts to reverse engineer the circuitry. Sensitive circuits may also be divided among the layers in such a way as to obscure the function of each layer.

Bandwidth - 3D integration allows large numbers dice to be stacked on each other and properly interconnected via dedicated set of wires (see Figure 1.1.2). This allows construction of wide

bandwidth buses between functional blocks in different layers. A typical example would be a processor plus memory 3D stack, with the cache memory stacked on top of the processor. This arrangement allows a bus much wider than the typical 128 or 256 bits between the cache and processor. Wide buses in turn alleviate the memory wall problem.

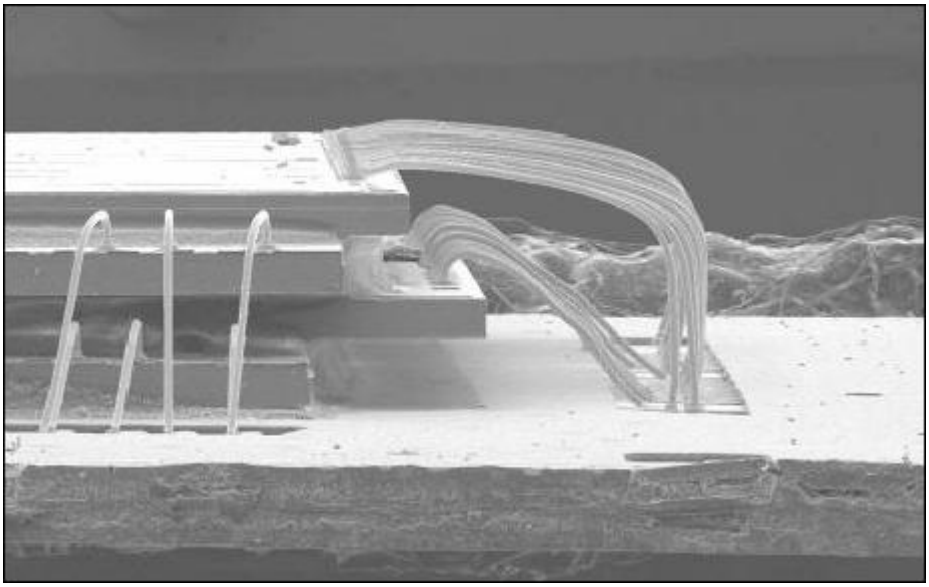

Figure 1.1.2 Detail of electrical wires between dice

A key role in such a system is played by the physical channel (PHY), responsible for guaranteeing the required bandwidth and communication performance. Classical electrical channels are affected by physical issues limiting them, so novel solutions need being investigated in order to overcome such limitations. Current bandwidth requirements are of the order of 8Mb/s, but they are destined to increase for future systems.

In this proposal we explore, develop and demonstrate novel nano-scale plasmonic system-in-package interconnects. Two schemes will be implemented and tested for their functionality.

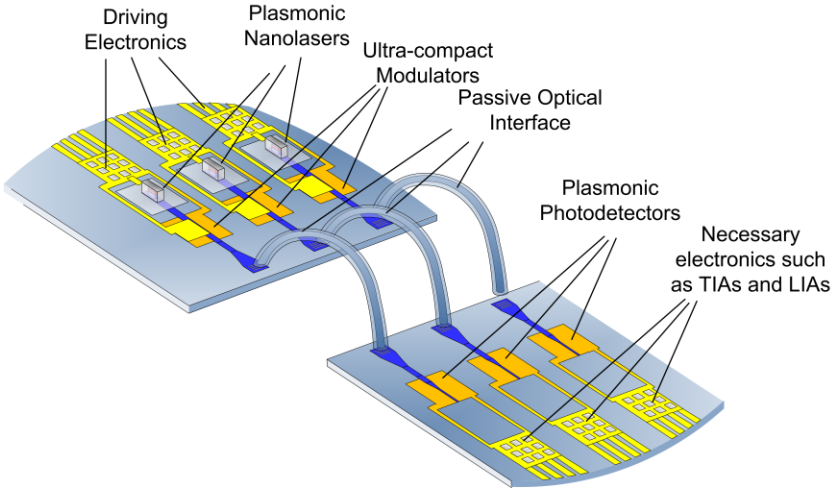

Figure 1.1.3 Interconnection of two CMOS chips with plasmonic lasers, photodetectors, fibers, amplifiers and drivers can be seen.

A first scheme is shown in Figure 1.1.3. The plot shows how two CMOS chips can be interconnected to each other exploiting a PHY interconnection based on plasmonic components, such as a LASER emitter, a photodetector and fiber arrays (note: fiber arrays may be used, yet project partner KIT has recently demonstrated new fiber bonds that allow point-to-point waveguide interconnection from one chip to another with wires 10 µm in width and up to several 100 µm in length). The picture also shows how potential necessary electronic laser drivers, trans-impedance amplifiers can directly be cointegrated with CMOS electronics.

Figure 1.1.4 shows a different type of interconnection of the two chips; instead of lying on the same plane and getting connected by a waveguide, in this case they are stacked on each other, and optical communication can happen to be free space, with no need for a guiding medium.

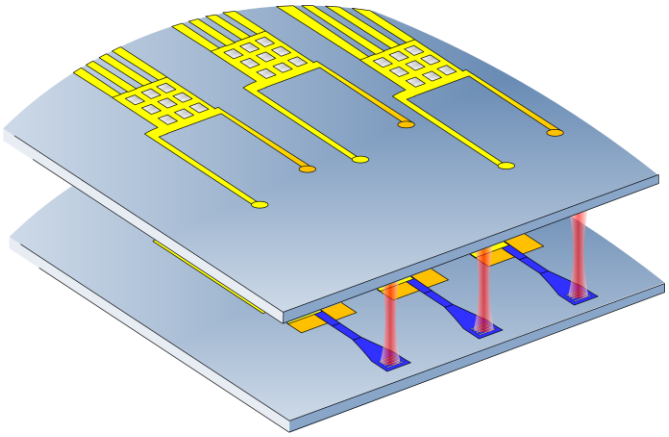

Figure 1.1.4 Concept of free space Interconnection of two CMOS chips with plasmonic lasers, photodetectors, fibers, amplifiers and drivers.

The research in plasmonic area has widely drawn attention in recent years [2] [3] [4], where the manipulation interaction of light and surface electrons at a metal-dielectric boundary and to develop techniques that can greatly localize optical fields below 100 nm for practical implementation of nano-scale photonic system devices of size tens of times shorter than the optical wavelength. Such devices are expected to require 100 times lower energy than conventional devices by exploiting quantum phenomenon and also have the capability for ultra wide bandwidth operation more than 100 GHz. However, these plasmonic devices suffer from high insertion loss due to metal induced attenuation, which can be compensated by introducing additional plasmonic waveguides integrated gain media and have been recently shown to exhibit enhanced propagation lengths by direct optical amplification in the telecommunication wavelength range[5], [6]. The Silicon-on-insulator (SOI) photonics platform is

[2] Jon A. Schuller, Edward Barnard, Wenshan Cai, Young Chul Jun, Justin White, and Mark L. Brongersm, "Plasmonics for extreme light concentration and manipulation," Nature Materials 9, 193-204 (2010)

[3] R. Zia, J.A. Schuller, A. Chandran, and M.L. Brongersma. "Plasmonics - the wave of chip-scale device technologies," Materials Today, vol. 9 (2006), 20-27.

[4] R.M. Briggs, J. Grandidier, S.P. Burgos, E. Feigenbaum, and H.A. Atwater, "Efficient Coupling between Dielectric-Loaded Plasmonic and Silicon Photonic Waveguides", Nano Letters 10, 4851-4857 (2010).

[5] Ambati, M., Nam, S. H., Ulin-Avila, E., Genov, D. A., Bartal, G. & Zhang, X. Observation of Stimulated Emission of Surface Plasmon Polaritons. Nano Letters 8, 3998–4001 (2008

[6] J. Grandidier, G. Colas des Francs, S. Massenot, A. Bouhelier, L. Markey, J.C. Weeber, C. Finot, and A. Dereux, "Gain assisted propagation in a plasmonic waveguide at telecom wavelength", Nano Letters 9, 2935-2939 (2009)

emerging as the standard technology for optical systems on a chip. The integration with SOI can facilitate the realization of on-chip plasmonic devices that will maintain all the advantages of plasmonic effect, while SOI waveguides can serve as low-loss interconnects for optical data transport between miniaturized plasmonic devices, thus minimizing overall on-chip losses.

The concept of this project is to develop a prototype interconnection platform to replace the current electronic data transfer technology within and around processors, high speed memory access and data centres operating at the rate of 100 Gbit/s with the world's first smallest size silicon photonics interface in the order of sub-micrometer. This concept will be realized by developing several breakthrough and disruptive plasmonic technologies in several areas including light emission, guiding and transporting it within the silicon waveguide, encoding optical carriers, amplification of signals, coupling from and to Si waveguide, detecting modulated optical signal, other necessary passive photonic components and finally integration of all developed devices to demonstrate real chip-to-chip interconnection application running at the data rate of 10-100 Gbit/s.

B1.1.2. *Project Objectives*

The objectives of the NAVOLCHI project are as follows:

Objective 1: Development of Transmitter

The transmitter chip consists of an electrically pumped hybrid plasmonic InP laser on a silicon waveguide structure and a plasmonic Si based modulator to externally encode data at the rate of up to 100 Gbit/s. The small footprints of both plasmonic laser as well as modulator make their combination perfect for realization of an optical transmitter chip with dimensions comparable to electronic devices. Thus, it will be possible to build several tens to hundreds such Si based transmitter modules integrated together using standard high-volume, low-cost silicon CMOS manufacturing technologies in order to produce low-cost, ultra small size photonic chips. This kind of plasmonic compact transmitter chip can be a solution for high speed, low cost interconnection between various electrical chips. In addition the breakthrough dimensions of the plasmonic laser and modulator create a possibility to efficiently combine clusters of plasmonic transmitters on the same chip. Replacing the electrical interconnects from current electrical chips with high speed plasmonic interconnects becomes possible without significantly increasing the footprint of the electrical chip.

Objective 1a: Development of Ultra-Compact Plasmonic Lasers with up to milliWatt Power Output

We have built up considerable expertise in electrically pumped metallic and plasmonic nano-lasers. The method of constructing these devices involving encasing nano-scale semiconductor gain medium in metal structures, has special merits: unprecedented high electrical pumping densities, large overlap of the photonic field with the active material, very efficient heat removal. These merits combined with a short photon lifetime will allow these devices to have Terahertz modulation speed at low electrical power. In the project we will study how this technology can be applied to Si wafer bonded laser sources. We will

use the mature heterogeneous III-V on silicon integration platform developed by IMEC. Note that the compatibility of this platform with processing in a CMOS line was recently demonstrated [7], [8].

The objectives related to the development of SOI bonded plasmonic lasers are as follows:

(1) Defining the optimum size and layer structure of the laser to obtain maximum output power into either a plasmonic or conventional SOI waveguide.

(2) Fabricate electrically pumped plasmonic/metallic nano-laser devices bonded onto an SOI wafer with light coupled into either a plasmonic or conventional SOI waveguide.

(3) Performance targets for the laser are an active region area less than approximately one square micron, and optical output power coupled into the waveguide of at least approximately 100 microwatts with an attempt to achieve output powers up to one milliwatt.

The target objective of ultra-compact plasmonic lasers will be realized in task 3.4 in Work Package (WP)-3.

Objective 1b: Development of Ultra-fast and Small Plasmonic Modulators

This objective deals with the realization of surface plasmon polariton based modulators with a large operational bandwidth. Both electrical and optical strong field confinements in metal-insulator-metal (MIM) structures enhance all physical effects that by now have been responsible for the optical signal encoding such as plasma, electro-absorption and linear electro-optic effects. Consequently, the size of the active optical components can be significantly reduced using such plasmonic waveguides. We aim to reduce the characteristic dimensions of optical modulators down to several micrometers in length, therefore, paving the way for ultra-compact optics with dimensions comparable to electronic components. In addition, electrically active plasmon devices gain several advantages from their conventional counterparts that the same metallic electrode are used for both optical and electrical waveguiding thus the fabrication is void of any kind of additional treatments such as e.g. n and p-type doping. Moreover, because of possible ultra-compact dimensions, the matching of the group velocities of both electrical and optical signals becomes unnecessary. Ultrafast performance of the modulator can be supplied from the metal itself due to the fast electronic transition in it or from the linear-electro optically active organic polymers sandwiched between two metallic electrodes.

The objectives relating to the development of plasmonic modulators will be:

(1) More than 3 dB extinction ratio in devices shorter than 10 μm will be demonstrated.

(2) Modulation speeds up to 40Gbit/s and higher will be demonstrated.

The target objective of small plasmonic modulators will be realized in WP-3.

[7] D. Van Thourhout, Photonics Europe, Brussels 2010

[8] Keynote talk INTEL at ACP

Objective 2: Development of Receiver technology

The objective to develop a receiver for chip-to-chip interconnection is to measure light under low input power level conditions. Such a receiver will potentially comprise of a plasmonic optical amplifier in order to deliver appropriate signal level to the on-chip detector and a photodetector for a signal at the specific wavelength with a footprint comparable to the other devices developed on the chip.

Objective 2a: Development of Plasmonic Optical Amplifier Based on Colloidal Nanocrystals

To enhance the sensitivity of the receiver, we will develop a plasmonic amplifier using IV-VI colloidal quantum dots (QDots) as the gain medium. These QDots are able to produce photons at telecom wavelengths with high internal quantum yield. Plasmonic effects will be used to maximize the confinement of the energy in the gain region. We will investigate two basic structures, one based on using a gold nanowire to confine the light and one using a hybrid silicon-plasmonic waveguide. Initially the structures will be optically pumped, but we will also investigate suitable electrical injection schemes and the final goal is a very compact fully electrically pumped optical amplifier.

The objectives relating to the development of the optical amplifier based on colloidal nanocrystals will be:

(1) 10dB on-chip gain for QDot based plasmonic amplifier

(2) Electrical injection of QDot based plasmonic amplifier

The target objective of developing plasmonic amplifier will be realized in WP-4.

Objective 2b: Development of a Fast Plasmonic Photo Detector

A plasmonic photodetector should be able to measure SPP signals coming from different plasmonic waveguide channels on the same chip or a second connected chip that converts plasmons into photons or into an electrical signal. A different concept may be used if needed to directly measure photons but using plasmonic approaches to increase responsivity and reduce the final footprint of the final device. Both concepts can make use of colloidal QDs eventually embedded into conductive polymers to define micrometric photodetectors on Si substrates or directly into nano-gaps between metal nanocontacts.

The objectives relating to the development of plasmonic photodetectors will be:

(1) Photon-plasmon conversion

(2) Quantum efficiencies above 80 %

(3) Responsitivities above 0.1 A/W).

The target objective of developing fast plasmonic photo detector will be realized in WP-4.

Objective 3: Development of plasmonic passive components

Objective 3 deals with the realization of the key optical passive components such as optical gratings, optical filters and plasmonic couplers to be employed in plasmonic transmitter and receivers.

Objective 3a: Development of plasmonic waveguide couplers

Both for the optical modulator and the optical amplifier we need to couple efficiently light from a standard silicon waveguide – which is used for transporting the signals over the chip -to a highly confined plasmonic waveguide – which is used for realizing ultra-compact and efficient active devices. In particular we will demonstrate metallic taper and direction couplers for light coupling from silicon nanowire into the plasmonic MIM waveguides used for realizing the modulator with a coupling efficiency exceeding 35%. We also aim at designing efficient coupling towards the hybrid silicon-plasmonic waveguides used for the optical amplifier.

The objectives relating to the development of plasmonic waveguide couplers will be:

(1) A plasmonic coupler for coupling into a plasmonic slot structure with dimensions of 50-100nm, with > 30% coupling efficiency.

(2) A plasmonic coupler for coupling into a hybrid silicon-plasmonic waveguide structure, with > 30% coupling efficiency.

The target objective of developing a plasmonic waveguide coupler will be realized in WP-5.

Objective 3b: Development of Beam Shaping Couplers that allow free-space optical interconnects to another chip.

Within the project we want to couple optical beams between different chips in the MCM-package. Standard edge coupling (no access) or standard surface grating couplers (to strongly diverging) cannot be used for this purpose. Therefore we will investigate and demonstrate approaches for shaping the beam emitted through the surface of a silicon waveguide chip, either using specially adapted surface grating couplers or using sub-wavelength diffractive grating structures inserted between both chips.

The objectives related to the development of beam shaping couplers are:

(1) Design beam shaping structures for coupling light between two chips at distance larger than 1mm, with bandwidth > 10nm and efficiency > 3dB

(2) Fabrication and characterization of such structures

The target objective of developing beam shapers will be realized in WP-5.

Objective 3c: Development of ultra-compact optical filters

We will develop a compact optical filter to cancel out the noise of the optical amplifier. The objectives related to the development of the optical filters are:

(1) Optical filter with 3nm bandwidth, 10dB suppression, 30nm free spectral range

The target objective of developing compact filters will be realized in WP-5.

Objective 4: Benchmarking in Reference to other Technologies

The consortium will benchmark the new plasmonic interconnect technology against other reference interconnect technology for highest speed such the Intel LightPeak approach or the Luxtera BLAZER approach.

The measurable results from the successful implementation of this objective will be

(1) Report on benchmarking.

(2) From a system point of view, a benchmarking between the communication within a System in Package (SiP) implemented via a dedicated dual dice communication module (DDCM) with a traditional electrical physical layer (PHY) and the novel plasmonic interconnect will be carried out as well. While a complete, even though simple, SiP can be implemented with the CMOS technology currently available as well as with the technology forecasted in a 3 years time frame, the implementation of a SiP exploiting plasmonic interconnect looks a quite far possibility mainly because of technology limitations. For this reason the validation in terms of performance of the plasmonic interconnect will be carried out exploiting as inputs data coming from netlist simulation of the CMOS chip, and on the opposite the plasmonic interconnect out data will be fed back to the simulated CMOS chip netlist. Plasmonic interconnect benchmarking will be then performed by means of cosimulation of CMOS chip netlist and plasmonic interconnect actual devices. An alternative possibility is to implement the CMOS chip in FPGA form and connect electrically FPGA IO to plasmonic interconnect devices IO. Carrying out this activity cannot be guaranteed at the moment with the current vision of required versus achievable performance and physical needs.

(3) The system integration of the chip-to-chip interconnects and its performance evaluation will be performed in task 6.5 & 6.6 in WP6. And, the benchmarking with respect to other technology will be provided in task 2.4 in WP2.

B1.1.3. *Relevance to call objectives*

NAVOLCHI addresses the ICT **Challenge 3: Alternative Paths to Components and System** of the FP7 framework. NAVOLCHI makes use of plasmonics in order *to miniaturize high speed photonics* for *small footprint optical interconnects*. The ideas within NAVOLCHI will lead to an *electronic compatible silicon photonic technology*. The ultra-small size of the plasmonic devices proposed by NAVOLCHI pave the way to large scale integrated plasmonics circuits and allows operation of many transmitters in parallel. It is the hope of the proposal that the efforts will pave the way to an *ultra-fast multicore computing area*.

NAVOLCHI focuses on meeting the prime goals and expected impacts of the objective **ICT-2011.3.5(b) Core and Disruptive Photonic Technologies** of the FP7 work programme. Particularly, NAVOLCHI meets the two targets *objectives* and *set of outcomes* of "disruptive photonic technologies" and "core photonic technologies":

Disruptive photonic technologies

NAVOLCHI aims to put its best effort on the development of a *new Si-plasmonic technology* for chip-to-chip interconnection. The proposed Si-plasmonic technology relies on ultra-compact and high-performance plasmonic components that currently are at a *proof-of-principle* stage but potentially offer a *breakthrough advances in functionality, performance, component size and cost reduction*.

The objective of NAVOLCHI is to expand and increase activities in the development of these devices and - as a final goal - to *bring them from the research lab closer to applications*, by demonstrating their industrial potential through a functional component.

NAVOLCHI is driven by industrial requirements and has the support and involvement of one of Europe's premier semiconductor fab: ST Microelectronics. ST Microelectronics will validate results for the optical interconnect applications.

The key plasmonic components investigated by NAVOLCHI are:

Plasmonic nano-laser — The most compact, cost effective high performance laser source outperforming all the state of the art solutions. The laser is capable of operating with up to 1 mW output power.

Plasmonic modulators — One of the smallest high speed modulators with straight forward fabrication requirements (more than 3 dB extinction ratios)

Plasmonic amplifier — QD based gain for SPP propagation on quasi-1D metal waveguides

Plasmonic photodetector — A small footprint and highly sensitive solution for small light signal or direct SPP detection, depending on chip configurations.

Core Photonic Technologies

NAVOLCHI proposes *economical integration of electronics/photonics* via making use of the plasmonics as unique bridge between these two technologies. NAVOLCHI will provide new

opportunities for advanced products, with a view to industrialisation. The plasmonic components particularly, their combination makes NAVOLCHI approach "breakthrough".

The application area of NAVOLCHI covers the two application fields:

- Optical data communications: Optical interconnects

  NAVOLCHI will demonstrate *high speed and cost efficient plasmonic interconnects.* Due to the strong optical field confinement in active region of plasmonic nano-laser, the technology developed by NAVOLCHI shows also a strong potential for being an energy efficient solution for future high speed chip-to-chip interconnects. The speed of the plasmonic interconnects proposed by NAVOLCHI is capable of *exceeding the 100Gb/s* range and managing data rates up to the *Tb/s region*. NAVOLCHI will bring a prototype laser to applying in a real application e.g. optical interconnects for super computing

- Photonic integration platforms

  The approach of NAVOLCHI relies on the employment of ultra-compact Si-plasmonic components that are several orders of magnitude smaller in their footprints than their photonic counterparts ensuring the *scalability for new technology generations*. The approach enables *automated high volume manufacturing* of *high speed* and *high performance Si-plasmonic* devices parallel to electronics which will significantly reduce the cost per function. Combining the scientific ideas with the industrial partner NAVOLCHI present a credible *route to industrial manufacturing in Europe*.

In addition, NAVOLCHI activities extend over the objective: **ICT-2011.3.1 Very advanced nano-electronic components: design, engineering, technology and manufacturability** of the FP7 work programme.

NAVOLCHI not only proposes new ideas that have capabilities of outperforming current state of the art solutions, but also addresses to their application in current electronics. It aims to link new advanced plasmonics component technologies with advanced system design to support *miniaturised electronics*. The technology covered by NAVOLCHI fulfils the criteria of *"systemability", "integratability" and "manufacturability"*. Plasmonic nano-laser and modulators proposed by NAVOLCHI can be irreplaceable parts of future high speed *switches and interconnects* that offer scalability and good performance. The similarities between electronics and plasmonics – both have comparable characteristic dimensions as well as make use of metals for current and light manipulation respectively – ensure their *ease and economical manufacturability* on the same chip. After all, *the nano-plasmonic & interconnects can easily be integrated with nano-CMOS technology.* NAVOLCHI device can be potentially utilized in information displays, lighting, and memory and storage application.

Required performance estimation

The plasmonic interconnect required performance is strongly based on the expectations from System in Package technology.

An analysis carried out in ST on the benefits of the System in Package approach shows that the overall computation capability of all the modules placed in a die of a CMOS system will be in the order of Tera-operations/s, thanks to multi-core architectures enabled by the nanometer technologies. In the

case in which traffic sources and destinations are physically placed on different dice, the corresponding traffic, originating a **bandwidth requirement**, quantifiable in the order of Tera-bits/s has to be managed by the die-to-die plasmonic interconnect.

The **number of optical links** between the dice depends of a number of factors:

(1) Bandwidth requirement – high bandwidth can be obtained parallelizing optical transmission between dice.

(2) Cost of plasmonic emitters and detectors – data serialization allows to reduce the number of emitters and detectors, even if at the price of a reduced bandwidth.

(3) Number of traffic sources in a die requiring to access simultaneously resources in another die – when traffics from different sources can be concentrated because simultaneity is not required, the number of optical links can be reduced.

(4) A compromise has to be found between velocity versus space division multiplexing.

Such a number depends then on architectural choices done on the system during the specification phase.

The **length of an optical link** (waveguide) depends on the distance between adjacent dice. This can be controlled in the context of packaging process. In case of TSV technology used for 3D integration, the depth of a via ranges from tens microns to 100/150 microns, but dice are stacked on each other with negligible spacing among them. This means that the length of an optical waveguide can be, theoretically, the smallest possible.

The **driving voltage** should be in the order of 1-1.5 v (peak-to-peak).

Scalability: the technology will be shown for two chips, but possible concepts for many interconnects will be addressed even though not demonstrated.

Besides the Chip-to-Chip interconnection platform, exploitation of additional applications will be considered, e.g. optical on-chip interconnects and implementation of 3D concepts. However, these additional applications will not be considered as direct goals, but shall be pointed out as possible pathways for future research during the project.

B1.2. Progress beyond the state of the art

B1.2.1. *Progress beyond the state of the art- with respect to chip-to-chip interconnection*

A number of technology options compete in the chip-to-chip interconnect space. To outline the state-of-the art and related issues we here examine the four most prominent chip-to-chip solutions: PCI express the STBus-based SHOC/SPA, RapidIO and HyperTransport. A summary of key features across the technologies is presented as follows

B1.2.1.1. PCI express (PCIe)

PCIe is an extension of the traditional PCI standard. The parallel shared bus is replaced by point to point links (lanes) implemented over a high speed serial interface. PCIe defines the physical, datalink and transaction layers. The bandwidth of a PCIe link can be scaled in bandwidth by adding lanes to a link.

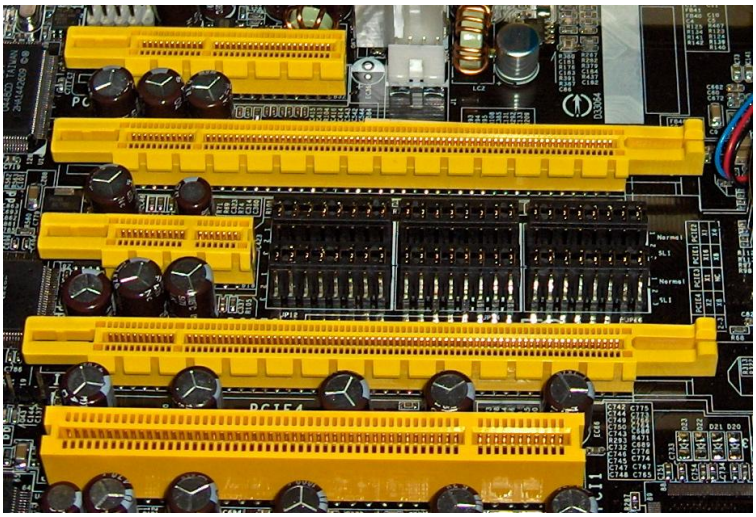

Figure 1.2.1PCI express slots

As with PCI access between devices are DMA initiated, which implies a software process to sequence these data moves. Since the majority of IP implemented on the Grommet device is DMA based an amount of buffering would be required locally in order for the data to be exchanged between the IP controller and the PCIe controller.

PCI interrupts are not implemented as sideband signals in PCIe; they are passed across links as part of the data flow (e.g. door-bell model).

The physical layer implements 8b10b encoding in order to embed a clock signal into the data, this implies a 25% overhead at the physical layer. This must be taken into account when determining system performance.

PCIe packets range between 4Bytes and 4KBytes in size, with an overhead of (16 + 8) bytes.

The DMA based model does not scale easily to connecting multiple devices together; since native routing is not supported by the protocol intermediate stages are required in order to forward transactions across an interconnect constructed from PCIe.

Field Programmable Gate Array (FPGA) devices with PCIe PHYs are available.

B1.2.1.2. SHOC / SPA

SHOC (SuperHyway Off-Chip) and its successor SPA (STBus Prototyping Aid) extend STBus / STNoC (STMicroelectronics on-chip interconnect solutions) off chip by reducing the interface width and multiplexing request and response virtual channels on to two unidirectional physical links. The primary function of this technology is to enable silicon/FPGA hybrid system prototyping.

By natively forwarding STBus/STNoC packets using SHOC/SPA incurs no software overhead, the system routers simply need to be configured with the appropriate address map in order to route requests to IP located across the SHOC/SPA.

All STBus protocol packets are supported natively. The SHOC provides limited support for interrupt and power-down interfaces.

SHOC/SPA does not mandate a physical layer, current implementations (e.g. SH4-202 eval chip) utilize standard TTL logic pads, and therefore the choice of physical layer is open.

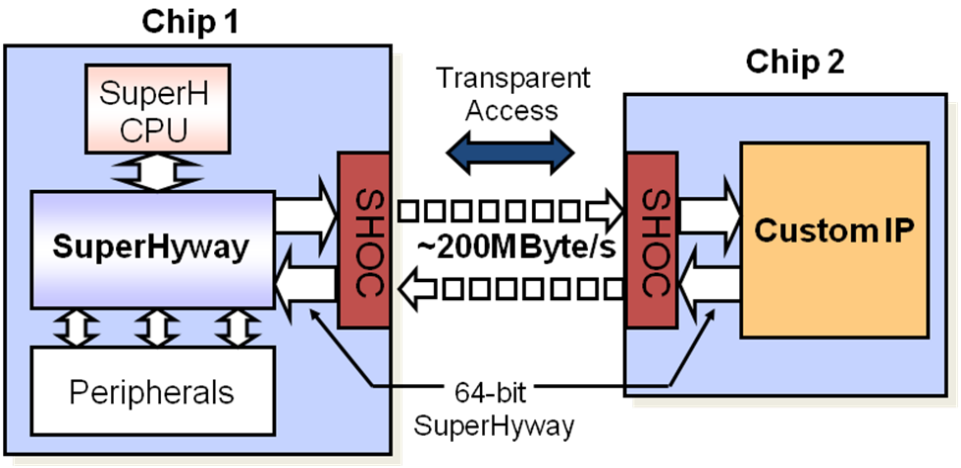

Figure 1.2.2 SHOC utilization example

B1.2.1.3. RapidIO (serial)

RapidIO is an 'open specification' interconnects aimed at connecting multiple devices in embedded systems. It implements many of the features found in packet switched fabrics; for example, QoS, multicast, reliability and so on.

The standard defines a physical layer operating at 1.25 / 2.5 / 3.125 Gbaud/s using the XAUI PHY.

The use of XAUI implies that 8b10b encoding is used in order to embed the clock within the data on the serial links this implies a 25% overhead at the physical layer.

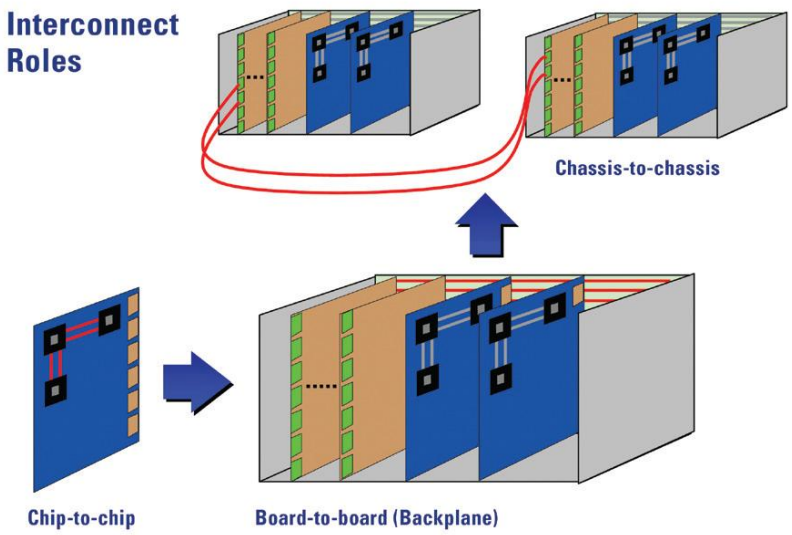

Figure 1.2.3 RapidIO interconnects usage

RapidIO supports a message passing protocol for mailbox / doorbell schemes. Data streaming modes are supported.

The RapidIO specification defines payload data to be big-endian formatted. This likely implies that an endianess conversion would be needed at either side of the link.

Each packet is acknowledged at the physical layer; however some transactions can be posted for example, at the logical layer.

Scaling in number of agents in a RapidIO interconnect is straightforward due to the packet switched nature of the specification.

FPGA devices are available with RapidIO interfaces are available on the market.

B1.2.1.4. HyperTransport

HyperTransport is an 'open specification' aimed at the microprocessor market where it is used as a replacement for the traditional 'front-side bus' on CPUs as well as for creating multiprocessor computers. It is a packet based network supporting interrupt passing, management protocols etc.

The physical layer does not embed the clock within a serial data stream (in contrast to PCIe and RapidIO) and so does not incur a physical layer bandwidth overhead normally associated with this.

Using a 2.5v LVDS/DDR like physical layer per lane bandwidth is 6.4 Gbit/s. The HyperTransport can be optimized for latency by defining packet payloads to be between 4 and 64 bytes in size.

Support for hardware discovery and power-management is provided by integrating the Advanced Configuration and Power Interface (ACPI).

The **NAVOLCHI optical chip-to-chip interconnect solution brings progress beyond state-of-the art by overcoming both performance and technological issues**. Performance is expected to be enhanced thanks to the much higher bandwidth offered by light and plasmonic devices as described in

related dedicated sections, while from a technological point of view the possibility to put in touch two chips through light beams either directly or via optical waveguides (fibers) would remove all the issues linked to wire bonding or TSV (Trough Silicon Vias) connections.

Special Features	HT 1.x	HT 2.0	HT 3.0	HT 3.1
Max Clock Speed	800 MHz	1.4 GHz	2.6 GHz	3.2 GHz
Max Aggregate Bandwidth (32-bit links)	12.8 GB/s	22.4 GB/s	41.6 GB/s	51.2 GB/s
AC Operation – Capacitive Coupling (optional) with AC/DC Autosensing, Autoconfiguration	No	No	Yes	Yes
Link Splitting (un-ganging) Each HT Link Split into 2x Half-Width Links	No	No	Yes	Yes
Hot-Plugging	No	No	Yes	Yes
Dynamic Link Clock/Width Adjustment	No	No	Yes	Yes
DirectPackets™ Data Streaming - +16 Virtual Channels (22 total), Peer-to-Peer Support, Native Packet Handling	HT 1.1 only	Yes	Yes	Yes
PCI Express Mapping	No	Yes	Yes	Yes
Common Features				
2 x Unidirectional, Low-Voltage-Differential-Signaling Links per HT Bus				
Scalable Link Width (2-bit to 32-bit)				
Asymetric Link Support (different link widths)				
Asynchronous Link Operation				
Clock Forwarding (no SerDes latency penalty)				
DC Operation (direct signal coupling)				
PCI, PCI-X Mapping				
Priority Request Interleaving™ (lowest I/O latency)				
Virtual Channels Support (6)				
Error Retry				

Figure 1.2.4 HyperTransport interconnects main features

B1.2.2. *Progress beyond the state of the art- with respect to state-of-the art Transmitters*

State-of-the art integrated lasers are either waveguide or VCSEL lasers. The former are several 100s of μm to a few millimeters in length or consume several 100 um^2 of space. Neither solution will allow optical chip-to-chip interconnect with several 100 connections. Limitations clearly are due to space, due to excessive power consumption and speed.

The situation is even worse for state-of-the art photonic modulators. They offer high-speed but their characteristic dimensions are limited by fundamental nonlinear interaction lengths. For instance, to this point the Lithiumniobate modulators still remains the most frequently used modulator for encoding optical signals with data rates of up to 40Gb/s [9]. They usually operate with more than 5V maximum voltage swing and have dimensions exceeding 1cm along the light propagation direction. Consequently, powerful electrical amplifiers are necessary for generating the electrical signal with a peak-to-peak large enough amplitude for driving the modulator. Thus, the Lithiumniobate solution is still costly, shows high power consumption and cannot be easily integrated with other optical circuits. Alternatively, electro-absorption modulators (EAM) belong to the most compact commercially available data encoding

[9] Avanex Powerbit SD-40, http://www.avanex.com

devices in optical communications. They are available in typical lengths of 200 μm and with operating speeds up to 40Gb/s. Unfortunately, junction capacities and carrier related effects fundamentally limit their bandwidth to approximately 60 GHz [10]. To overcome these limitations travelling wave configuration can be designed, which, however increases the device dimensions even more [11]. Last but not least, the EAMs usually relay on the InP platform, which is not really CMOS compatible making them economically challenging for a future mass market. More recently, CMOS compatible silicon solutions have been suggested [12]. High speed all silicon and silicon – organic hybrid modulators with lengths of few millimetres with speeds exceeding 40Gb/s have already been demonstrated [13],[14]. More compact Si based modulators have been demonstrated in resonant structures. Normally their operation is based on either the carrier injection effect or the carrier-depletion effect [15]. Unfortunately, the operating speeds of these more compact resonant silicon devices are ultimately limited by the finite mobility of the free carriers.

Therefore, all the state-of-the art photonic solution neither offers compact dimensions nor highest speed.

The NAVOLCHI proposal makes use of two elegant solutions – a recently proposed plasmonic nano-laser [21] and an ultra-compact high speed absorption/phase modulators – for realization of plasmonic transmitter with dimensions in the order of a few $1 \mu m^2$. Unlike to the full plasmonic approach NAVOLCHI makes use of silicon wire waveguides for on-chip communication and therefore significantly reducing the overall plasmonic losses.

B1.2.3. *Progress beyond the state of the art- with respect to plasmonic Lasers*

The last few years has seen the emergence of metallic and plasmonic nano-lasers. Most of these devices are optically pumped [16] [17] [18] [19]. However, we have been involved in developing electrically

[10] H. Fukano, T. Yamanaka, M. Tamura, and Y. Kondo, Very-low-driving-voltage electroabsorption modulators operating at 40 Gb/s, Lightwave Technology, Journal of **24**, 2219 – 2224 (2006).

[11] U. Westergren, Y. Yu, and L. Thylén, High-speed traveling-wave electro-absorption modulators, **6350**, 635004 (2006).

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[14] L. Alloatti, D. Korn, D. Hillerkuss, T. Vallaitis, J. Li, R. Bonk, R. Palmer, T. Schellinger, A. Barklund, R. Dinu, J. Wieland, M. Fournier, J. Fedeli, W. Bogaerts, P. Dumon, R. Baets, C. Koos, W. Freude, and J. Leuthold, Silicon High-Speed Electro-Optic Modulator, in *Group IV Photonics* p. ThC2 (2010).

[15] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, Micrometre-scale silicon electro-optic modulator, Nature **435**, 325–327 (2005). http://dx.doi.org/10.1038/nature03569

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[17] R. Perahia, T. P. Mayer Alegre, A. H. Safavi-Naeini, and O. Painter, "Surface-plasmon mode hybridization in subwavelength microdisk lasers", Appl. Phys. Lett. 95, 201114 (2009).

[18] R.F. Oulton, V. J. Sorger, T. Zentgraf, R-M. Ma, C. Gladden, L. Dai, G. Bartal, and X. Zhang, "Plasmon lasers at deep subwavelength scale," Nature 461, 629–632 (2009).

[19] M. A. Noginov, G. Zhu, A. M. Belgrave, R. Bakker, V. M. Shalaev, E. E. Narimanov, S. Stout, E. Herz, T. Suteewong, and U. Wiesner, "Demonstration of a spaser-based nanolaser," Nature 460, 1110–1112 (2009).

pumped devices which is important for applications [20] [21]. In particular these electrically pumped devices have also been shown to work at room temperature, both in continuous and pulsed mode [22] [23]. All these devices have been made as standalone devices.

In this proposal we will move beyond single devices by bonding these devices to SOI wafers and then coupling the light output from these extremely small lasers into passive or plasmonic Si waveguides. This coupling to waveguides will greatly increase the usefulness of metallic/plasmonic nano-lasers. Figure 1.2.5 shows a schematic of our bonded nano-laser concept.

Another aspect of progress beyond the sate of the art we will address is to increase the output power levels of these devices, which are now at a few microwatts, levels of 100 microwatts to possibly one milliwatt.

To achieve these goals of efficient coupling and high optical output considerable simulation and design studies will also be performed. These studies will further knowledge on how best to employ metallic and plasmonic nano-laser in systems.

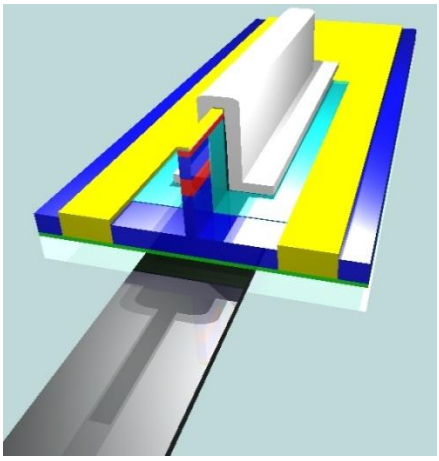

Figure 1.2.5 Structure of cavity formed by a rectangular semiconductor pillar encapsulated in Silver. This structure is then bonded onto an SOI wafer in which a Si waveguide has been made. Laser light in the rectangular pillar can couple into the Si wafer and be employed in the rest of the communication system.

[20] M. T. Hill, Y-S. Oei, B Smalbrugge, Y. Zhu, T. de Vries, P. J. van Veldhoven, F. W. M. van Otten, T. J. Eijkemans, J. P. Turkiewicz, H. de Waardt, E. J. Geluk, S-H. Kwon, Y-H. Lee, R. Nötzel, and M. K. Smit., "Lasing in Metallic-Coated Nanocavities," Nature Photonics 1, 589-594 (2007).

[21] M. T. Hill, M. Marell, E. S. P. Leong, B. Smalbrugge, Y. Zhu, M. Sun, P. J. van Veldhoven, E. J. Geluk, F. Karouta, Y-S. Oei, R. Nötzel, C-Z Ning, and M. K. Smit, "Lasing in metal-insulator-metal sub-wavelength plasmonic waveguides," Optics Express 17, 11110 (2009).

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[23] M. J. H. Marell, Dept. of Electrical Engineering, Technische Universiteit Eindhoven, Postbus 513, 5600 MB Eindhoven, The Netherlands, is preparing a manuscript on gap-plasmon mode DFB lasers in the near infrared wavelengths.

B1.2.4. *Progress beyond the state of the art- with respect to plasmonic Modulators*

Recently, plasmonic solutions have been explored more and more. A part of the community has put a focus on the realization of ultra-compact plasmonic modulators. Several approaches have been reported for modulating either the phase or the intensity of SPPs. Among these approaches the electrically operated ones are clearly of higher interest for practical applications. A technique proposed by Nikolajsen *et al.* [24] exploits the thermal effect in benzocyclobutene which limits the operating speed. The device by Dionne *et al.* [25] known as PlasMOStor device that exploits the carrier induced refractive index change in a silicon layer. In spite of its compact size, the operating speed in this device is limited by carrier mobility in silicon which makes its capability for high speed modulation still to be proven.

In contrast, the NAVOLCHI seeks to employ recently proposed two distinct plasmonic modulator approaches for a realization of full-functional ultra-compact high speed transmitter for the chip-to-chip interconnects [26,27]

- **CMOS compatible Surface Plasmon Polariton Electro - Absorption Modulator (SPPEAM)** has been reported to satisfy all the requirements for future low cost and high speed integrated circuits. It has been shown that 1dB extinction ratio is possible in the ultra-compact SPPEAM having a length of a few micrometer or even below 1μm. Being based on an electron screening effect in highly conductive metal-oxide layer the SPPEAM doesn't exhibit carrier related speed limitations and its operation is only limited by the *RC*-time constant of the device itself having a capacitance in a range of 1 femtofarad. Thus, operating speeds above *100Gbit/s* should be possible is the device length in the range of a *few micrometers*.

- **The modulation of SPP in the Mach-Zehnder interferometric (MZI) configuration** has previously been numerically demonstrated. It has been shown that, a combination of plasmonic nanoslot waveguide with nonlinear organic polymers show a great potential for a realization of Pockel's effect based plasmonic modulators. Providing as high speed as a silicon hybrid technology plasmonic approach reduces the length of the Pockel's effect based MZI modulators down to 20μm and below. Because of nanoscale distance between electrodes the necessary voltage swing of the driving signal to perform switching is significantly smaller, thus the power consumptions in these modulators is believed to be small. Moreover, fabrication simplicity of Metal-Insulator-Metal (MIM) based modulators on the other hand ensures its low cost and a fabrication process compatible with CMOS technology.
  Strong field localization in the plasmonic structures not only shortens the length of the optical modulators but also reduces the minimum distance between two neighbouring modulators with almost negligible cross-talk. The footprint of high speed optical modulators can be significantly

[24] T. Nikolajsen, K. Leosson, and S. I. Bozhevolnyi, Surface plasmon polariton based modulators and switches operating at telecom wavelengths, Appl. Phys. Lett. **85**, 5833–5835 (2004).v

[25] J. A. Dionne, K. Diest, L. A. Sweatlock, and H. A. Atwater, PlasMOStor: A Metal-Oxide-Si Field Effect Plasmonic Modulator, Nano Lett. **9**, 897–902 (2009).

[26] A. Melikyan, T. Vallaitis, N. Lindenmann, T. Schimmel, W. Freude, and J. Leuthold, "A Surface Plasmon Polariton Absorption Modulator", in *Conference on Lasers and Electro-Optics* p. JThE77 (2010).

[27] S.-I. Inoue and S. Yokoyama, Numerical simulation of ultra-compact electro-optic modulator based on nanoscale plasmon metal gap waveguides, Electronics Letters **45**, 1087–1089 (2009).

reduced following to these plasmonic approaches. Thus, plasmonic creates a possibility of efficiently combining cluster of modulators in the same chip.

B1.2.5. *Progress beyond the state of the art- with respect to plasmonic optical amplifiers*

Several approaches for providing gain on a silicon platform have been demonstrated in the last few years. The approaches are based either on silicon (INTEL, others) or III-V silicon hybrid technologies (UCSB, INTEL, IMEC). However, the amplifiers exploiting these approaches are bulky and power hungry, which makes them impractical for applications in optical interconnects. To realize a compact and power efficient amplifier, very high confinement of the light is required.

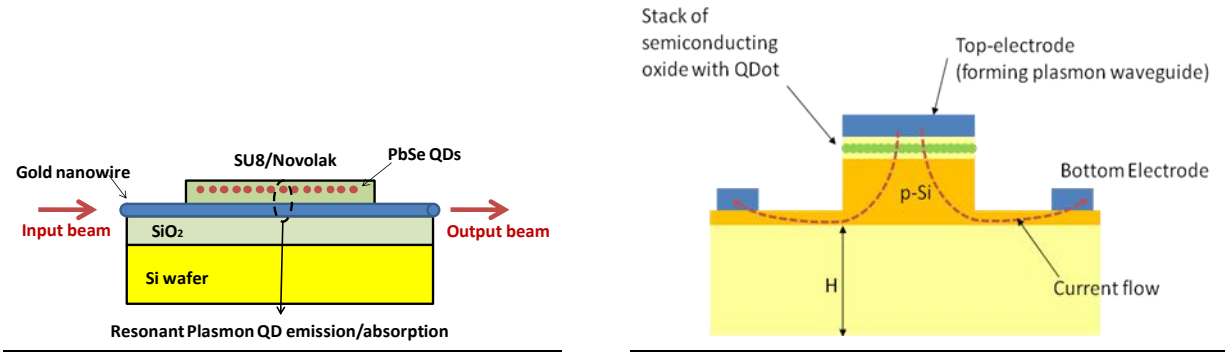

Figure 1.2.6. (Left) 1D SPP waveguide covered with a gain media based on PbSe QDs on UV patternable resists; (right) Hybrid silicon-plasmonic waveguide with gain produced by electrical injection.

Nanometallic or plasmonic waveguides have been considered for on-chip waveguiding in both single conductor and two-conductor configurations [28,29,30]. Such waveguides can strongly confine light to a very small (e. g., < 1 μm^2 scale) lateral area simultaneously causing an enhancement in a light-matter interaction. Clearly, in the absence of plasmonic losses these waveguides would have been perfect for light amplification with a very small pump power. Unfortunately, plasmonic waveguides usually are characterized by high losses (limiting propagation lengths in the order of several microns), which makes the amplification of SPPs challenging

In this project, an amplification of SPP is proposed (see designs in Figure 1.2.6), other than using short metallic waveguides. We will investigate electrically/optically pumped gain media providing a sufficient amplification at the telecom wavelengths, similar to the one recently demonstrated in visible and telecom wavelengths using 2D SPP propagation [31,32]. Proposed light amplification method will replace the transimpedance amplifiers typically used in the optical receivers.

[28] R. Zia, J. A. Schuller, and M. A. Brongersma, Near-field characterization of guided polariton propagation and cutoff in surface plasmon waveguides, Phys. Rev. B, vol. 74, p. 165415, 2006.

[29] G. Veronis and S. H. Fan, Modes of subwavelength plasmonic slot waveguides, J. Lightw. Technol., vol. 25, pp. 2511–2521, 2007.

[30] N.-N. Feng, M. L. Brongersma, and L. Dal Negro, Metal-dielectric slotwaveguide structures for the propagation of surface plasmon polaritons at 1.55 μm, IEEE J. Quantum Electron., vol. 43, pp. 479–485, 2007.

[31] Gather, M.C.; Meerholz, K.; Danz, N.; Leosson, K. Net optical gain in a plasmonic waveguide embedded in a fluorescent polymer, Nature Photonics 4, pp. 457-461 (2010).

B1.2.6. *Progress beyond the state of the art- with respect to plasmonic photo-detectors*

There have been recent demonstrations of very tightly integrated detector/transistor combinations using Ge on Si structures [33]. Ge is generally an interesting detector material because it has large enough absorption in the near infrared to allow photodetectors with micrometer sizes and it can be processed compatible with silicon [34]. A more advanced concept for low-capacitance and potentially high-speed photodetectors is to use nanometallic structures, such as antennas [35] and waveguides [36] to concentrate light into subwavelength active detector volumes. Some proof of principle and isolated devices utilizing surface plasmon polaritons have been build and they can be used in both active and passive optical interconnects components such as photodetectors, modulators and waveguides. They may also aid efficiency of classical light sources. At this very early phase of research, they are thought to have large potential for more exotic applications such as quantum computing because plasmonic technology can be used for building quantum light sources for single photons [37].

Nowadays organic technologies are unbeatable, more in price than in real performance. In this sense, organic materials combine high optical cross-sections, large and ultrafast nonlinear responses and broad spectral tunability (see for example Ref. [38] and others therein). If we combine these properties with lithographic processability [39], plasmonics [40] and quantum dots [41,42] many possibilities may be envisaged to develop sensitive photodetectors in many configurations and wavelength ranges, as will be demonstrated in the present project. Indeed, internal quantum efficiencies around 80% and responsivities around 0.16 A/W have been reported

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[32] Grandidier J, des Francs GC, Massenot S, Bouhelier A, Markey L, Weeber JC, Finot C, Dereux A., Gain-assisted propagation in a plasmonic waveguide at telecom wavelength, Nano Lett. 2009, 9, 2935-9.

[33] S. Sahni, X. Luo, J. Liu, Y. Xie, and E. Yablonovitch, B, Junction field-effecttransistor-based germanium photodetector on silicon-on-insulator, Opt. Lett., vol. 33, pp. 1138–1140, 2008.

[34] L. Chen, P. Dong, and M. Lipson, B, High performance germanium photodetectors integrated on submicron silicon waveguides by low temperature wafer bonding,Opt. Express, vol. 16, pp. 11513–11518, 2008.

[35] L. Tang, S. E. Kocabas, S. Latif, A. K. Okyay, D.-S. Ly-Gagnon, K. C. Saraswat, and D. A. B. Miller, Nanometre-scale germanium photodetector enhanced by a near-infrared dipole antenna, Nature Photon., vol. 2, pp. 226–229, 2008

[36] D.-S. Ly-Gagnon, S. E. Kocabas, and D. A. B. Miller, Characteristic impedance model for plasmonic metal slot waveguides, IEEE J. Sel. Topics Quantum Electron., vol. 14, pp. 1473–1478, 2008.

[37] D. E. Chang, A. S. Sorenson, E. A. Demler, M. D. Lukin,. A Single-Photon Transistor using Nanoscale Surface Plasmons. Nature Physics **3**. 807-812 (2007).

[38] J. Clark and G. Lanzani, Organic photonics for communications, Nat. Photonics 4, 438-446 (2010).

[39] R. Abargues, U. Nickel and P.J. Rodríguez-Cantó, Charge dissipation in e-beam lithography with Novolak-based conducting polymer films, Nanotechnology **19,** 125302 (2008).

[40] H. Ditlbacher, F. Aussenegg, J. Krenn, B. Lamprecht, G. Jakopic,, G. Leising, Organic diodes as monolithically integrated surface plasmon polariton detectors. Appl. Phys. Lett. **89**, 161101, (2006).

[41] T. Rauch, M. Boberl, S. F. Tedde, J. Furst, M. V. Kovalenko, G. N. Hesser, U. Lemmer, W. Heiss, and O. Hayden, Near-infrared imaging with quantum-dot sensitized organic photodiodes, Nat. Photonics **3**, 332 (2009).

[42] T.P. Osedach,_ S.M. Geyer, J.C. Ho, A. C. Arango, M.G. Bawendi, and V. Bulovic, **Lateral** heterojunction photodetector consisting of molecular organic and colloidal quantum dot thin films**,** Appl. Phys. Lett. **94**, 043307 (2009).

In the NAVOLCHI project two small footprint solutions for photodetectors compatible with CMOS technologies are envisaged as depicted in Figure 1.2.7, from a simple photoconductor based on IV-VI QDs into a nanogap between two metallic electrodes (left), up to a more complex concept based on conductive polymers with dispersed QDs and metal nanorods having a (longitudinal) localized surface plasmon resonant with the detection wavelength (1550 nm).

Two NAVOLCHI small footprint solutions for photodetectors compatible with CMOS technologies are depicted in Figure 1.2.7, from a simple photoconductor based on IV-VI QDs into a nanogap between two metallic electrodes (left), up to a more complex concept based on conductive polymers with dispersed QDs and metal nanorods having a (longitudinal) localized surface plasmon resonant with the detection wavelength (1550 nm).

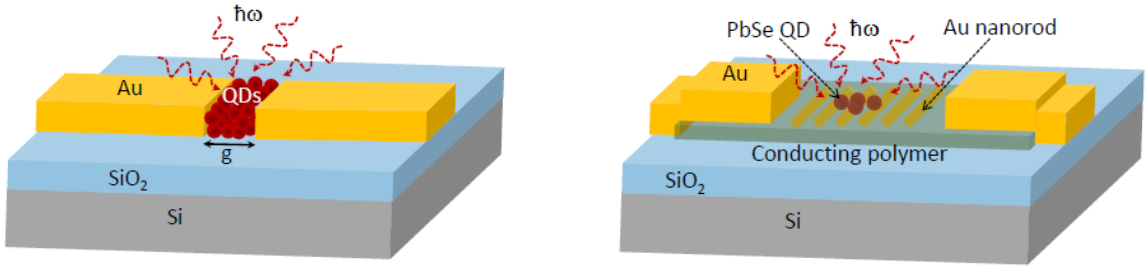


Figure 1.2.7 (left) Metal nanogap photoconductor containing QDs between electrodes with an effective absorption edge λ_g > 1.6 μm; (right) Photoconductor containing similar QDs plus metal nanorods whose length would resonantly couple light at telecom wavelengths.

B1.2.7. *Progress beyond the state of the art- with respect to plasmonic waveguide couplers*

Due to the high optical losses from metals, silicon wire passive waveguides are believed to be part of the plasmonic integrated circuits for on-chip communication. Thus, several approaches have been reported for light coupling from silicon nano-wire into the plasmonic, particular into the nano-slot plasmonic waveguides. It has been shown that broadband and highly efficient coupling can be achieved in the metallic tapered structures via funneling the light into the nano plasmonic waveguides. 35% coupling efficiency has been reported for the light coupling into the plasmonic waveguide with the slot size of 200nm [[43]]. Another coupling configuration has been reported by Delacour *et al.* [[44]]. The vertical direction coupler configuration between silicon wire and plasmonic slot waveguide has been experimentally investigated. The experiments have been accomplished for the plasmonic slot with dimensions of 100nm.

NAVOLCHI suggests using metallic tapering and hybrid direction couplers for light coupling into the plasmonic waveguides with slot dimensions in the range of 30-100 nm. Finite Integration

[43] J. Tian, S. Yu, W. Yan, and M. Qiu, "Broadband high-efficiency surface-plasmon-polariton coupler with silicon-metal interface", Appl. Phys. Lett. **95**, 013504 (2009).

[44] C. Delacour, S. Blaize, P. Grosse, J. M. Fedeli, A. Bruyant, R. Salas-Montiel, G. Lerondel, and A. Chelnokov, "Efficient Directional Coupling between Silicon and Copper Plasmonic Nanoslot Waveguides: toward Metal-Oxide-Silicon Nanophotonics", Nan. Lett. **10**, 2922–2926 (2010).

Technique (FIT) simulations have been carried out for the optimization of tapered metallic couplers. More than 80% coupling efficiency has been shown to be feasible by one of the applications group (KIT) and for slot size down to 50nm. We believe that it is possible to experimentally demonstrate more than 30% of coupling efficiency for 30-50nm plasmonic slots.

B1.3. S/T Methodology and associated work plan

The overall idea of the NAVOLCHI project is to exploit the possibilities offered by the new plasmonic silicon disruptive and hybrid approaches to demonstrate its versatility and superiority in a well defined realization for ultra small chip-to-chip communications platform. In the next paragraphs the detailed NAVOLCHI work plan is presented. According to this work plan the effort is split into seven lean work packages, see Figure 1.3.1.

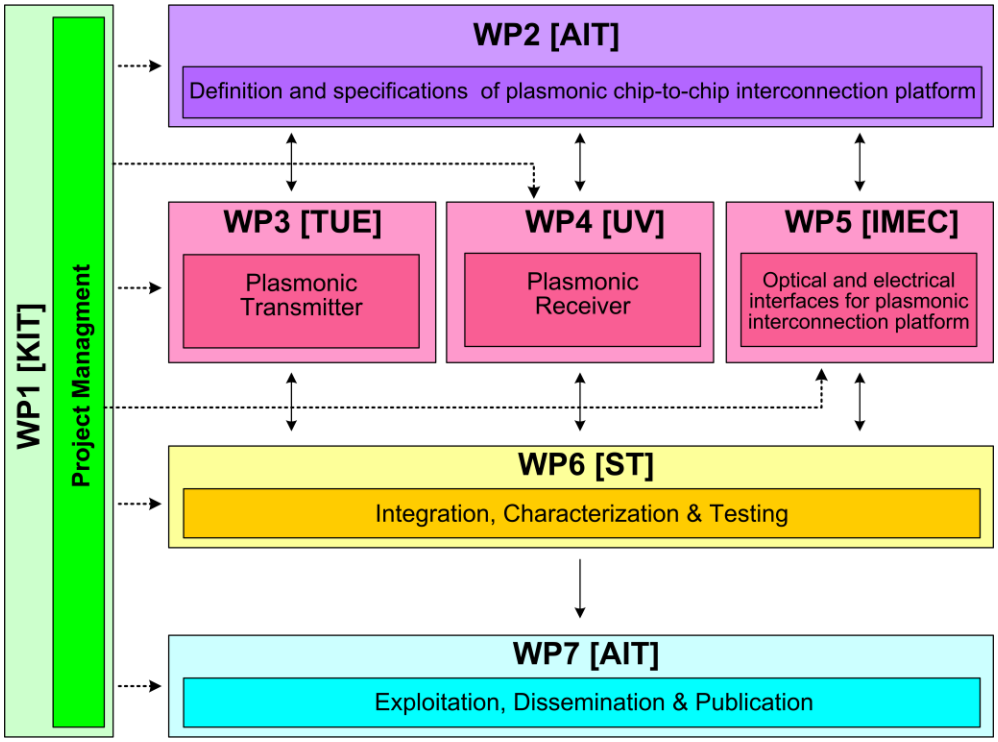


Figure 1.3.1 NAVOLCHI work-package and organization structures

B1.3.1. *Overall strategy and general description*

B1.3.1.1. Overall Work plan

The structure of the NAVOLCHI project is organized in seven work packages WP1 to WP7. The management of the project will be handled in work package WP1 and the exploitation and dissemination work package WP7 round up the overall organizational structure. The scientific and technical challenges and objectives of the project have been organized around five technical work packages. These are

WP2: This work package defines the plasmonic devices for chip-to-chip interconnects scenarios and specifies the related device and system requirements. High level modelling of the plasmonic devices is

forecasted as well in order to cosimulate CMOS circuits VHDL code and FE netlist with a PHY functional model. It interacts with the other work-packages in order to exchange information on material parameters and potentials interconnect performance. WP2 consequently also identifies new opportunities related to this new platform and makes sure that WP 6 takes early action in filing patents.

WP3: This work package deal with the design of disruptive plasmonic silicon transmitters chip and development of a CMOS compatible laser and modulators technology for the new Si-photonic approach. The WP exchanges vital device specification information with WP2 prior to a new design. The chips fabricated in this work package are passed on to WP6.

WP4: This work package is focused on disruptive plasmonic receiver that includes development of plasmonic QD polymer based photodetector and gain assisted disruptive waveguide structures with an organic material. The WP exchanges vital device specification information with WP2 prior to a new design. This work package interacts with WP2 prior to chip design and passed on to WP6

WP5: This work package works on the development of plasmonic passive photonic components and the required CMOS circuits (die to die communication module, emitter driver, trans-impedance amplifier, etc.) needed to realise full plasmonic optical interconnect platform for chip-to-chip interconnection and will target to fabricate Si waveguide to plasmonic waveguide couplers, Si steering waveguide couples with gratings and other components for the manipulation of advanced optical modulation formats and filters. This WP also interacts with WP2 with respect to material parameter information exchange and to communicate new developments and passed on to WP6.

WP6: This work package provides highest-speed 100 Gbit/s chip-to-chip interconnect platform and chip testing and characterization. Results from this work package are communicated to the dissemination and exploitation work package 6 as well to WP 2.

WP7: Results from WP3 to WP5 are passed on to work package 6, within which exploitation and dissemination activities are coordinated.

B1.3.1.2. Implementation Description of Innovations

The NAVOLCHI project comprises some challenging and highly innovative work packages. In this section we give an overview on the implementations and realizations of these special tasks. The intention of this section is to show credibility that our proposal is funded on solid initial investigations and that we are able to perform the ambitious objections. The technical descriptions of the implementation of innovations from all the work packages are given as follows.

Technical description of the implementation of innovations from WP3, Plasmonic Transmitter

This plasmonic transmitter consists of two main parts, a plasmonic/metallic nano-laser and a plasmonic modulator.

For this aspect of the WP, firstly, simulations will investigate a number of aspects of the laser: Efficient generation and output coupling of light to either free space or waveguides has to be investigated. In principle, there are designs of metallic cavity that can allow efficient generation of light. However, there is often a tradeoff between the size of device and maximum achievable efficiency of the light/Plasmon emitter. Such design tradeoffs need to be simulated and fabricated in addition to the study of coupling of

the photons or plasmons (if metallic waveguides are chosen) from the laser to either free space or waveguides.

Secondly, based on the simulation results and consideration of requirements for silicon wafer bonded light source, an epitaxial layer stack for the device must be chosen and grown. In parallel, suitable waveguide patterns are defined in an SOI wafer through advanced DUV lithography and etching. Next, the III-V epitaxial layers are bonded on the SOI-wafer, and their substrate is removed. Then the laser mesa's are patterned and etched into the remaining III-V epitaxial layer. The metallization scheme needs to be chosen and implemented to address the needs of heatsinking and also electrical pumping. The finished fabricate devices (both before and after bonding) need to be tested to see how high a temperature they can operate at. Furthermore the intrinsic speed at which they can operate needs to be examined. Predictions indicate that these small metallic lasers could possibly operate with intrinsic modulation bandwidths close to the terahertz regime [45].

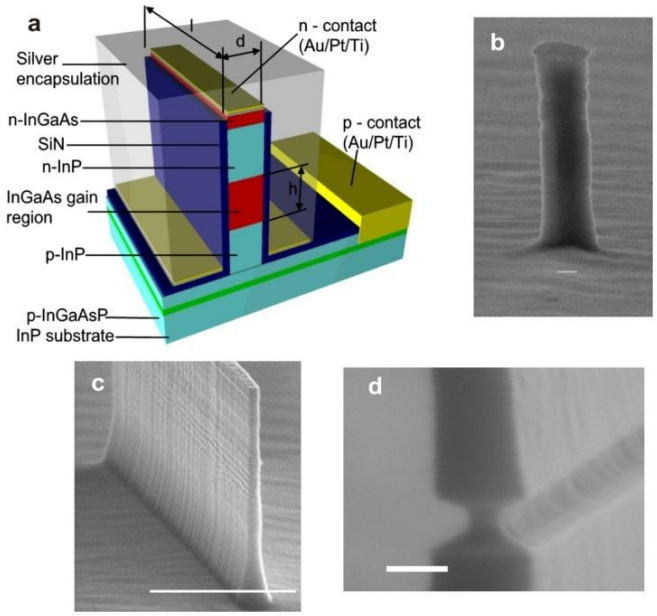


Figure 1.3.2 Structure of encapsulated hetero-structure laser device. In this case the semiconductor core has a thin rectangular shape to create a gap-plasmon mode waveguide. Other shapes are possible, including small round pillars. Some of the semiconductor core shapes possible are: b) round pillar structures, c) long thin rectangular structures for gap-plasmon mode waveguides. d) The waveguide can be indented in the centre to tightly confine the light in the vertical direction. All scale bars are 100nm, except for b) which is one micron.

For the **plasmonic modulator** part, two distinct SPP modulation approaches will be investigated during this project: One of the modulation approaches that NAVOLCHI targets is based on recently proposed new metal/metal-oxide/insulator/metal(MMoIM) structure[46,47]. It has been shown, that depending on the operating wavelength and thickness of the metal-oxide layer, either the phase or the intensity of SPP

[45] M. I. Stockman, "The spaser as a nanoscale quantum generator and ultrafast amplifier,"Journal of Optics A, 12, 024004, (2010).

[46] A. Melikyan, T. Vallaitis, N. Lindenmann, T. Schimmel, W. Freude, and J. Leuthold, "A Surface Plasmon Polariton Absorption Modulator", in *Conference on Lasers and Electro-Optics* p. JThE77 (2010).

[47] E. Feigenbaum, K. Diest, and H. A. Atwater, "Unity-Order Index Change in Transparent Conducting Oxides at Visible Frequencies", Nano Letters **10**, 2111–2116 (2010), pMID: 20481480.

at the MMoIM structure can be efficiently modulated by modulating the electron density of metal-oxide layer. Particularly, Indium Tin Oxide (ITO) has been shown to have suitable material properties for such a purpose. The feasibility of ITO to serve as an active layer for modulating either the phase or the intensity of SPP has already experimentally demonstrated for the test samples[47], [48].

Surface plasmon polariton absorption modulator (SPPAM**)** operating at 1.55µm communication wavelength has been proposed. This device operates based on the above mentioned four layer structure has been shown to have a potential for providing 1dB extinction ratio in the device length on the order of 1 µm and below [48]. SPPAM has been modelled integrated on the Si-technology. Photonic mode in silicon wire waveguide, see Figure 1.3.3(a), is coupled into the plasmonic mode (see Figure 1.3.3(c)) via hybrid mode in the directional coupler. The intensity of the SPP is subsequently modulated in the plasmonic active section with the length of *L*.

The feasibility of the SPPAM to be designed integrated on Si-technology has already been shown. Because of the high carrier mobility in highly conductive ultra-thin metal oxide layer, the modulation speed of device is theoretically limited by the *RC*-time constant of the device itself with the capacitance in the order of **1fF**, see Figure 1.3.3. Modelling will be performed to optimize the SPPAM for the NAVOLCHI application.

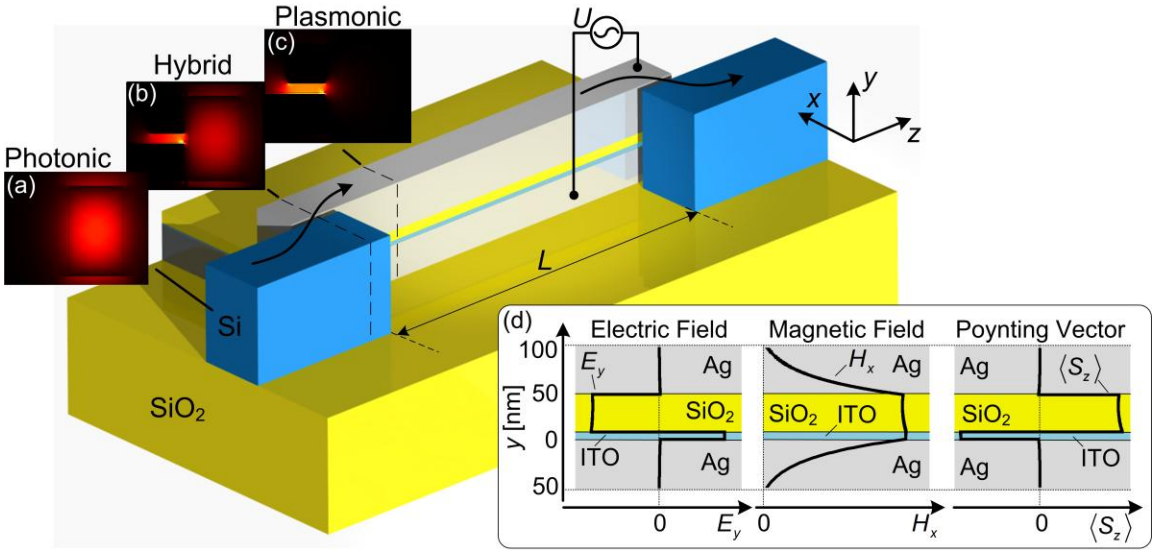


Figure 1.3.3 The structure of a surface plasmon polariton absorption modulator (SPPAM). Light is coupled from a silicon nanowire into an active plasmonic section by means of a directional coupler. The active section consists of a stack of silver (Ag), indium tin oxide (ITO), and SiO_2 layers. The absorption coefficient of the SPP is modulated by applying a voltage between the two silver electrodes. The insets show how a photonic mode (a) in a silicon strip waveguide excites a SPP (c) via a hybrid mode (b) in directional coupler. The insets in (d) show the electric field E_y and the magnetic field H_x as well as the time-averaged Poynting vector distributions The plot of the Poynting vector shows the power confinement of the SPP in the ITO layer. The length *L* describes the size of the modulator along the light propagation direction.

[1] [48] A. Melikyan, N. Lindenmann, S. Walheim, P. M. Leufke, S. Ulrich, J. Ye, P. Vincze, H. Hahn, Th. Schimmel, C. Koos, W. Freude, and J. Leuthold, Optics Express, Vol. 19, Issue 9, pp. 8855-8869, April 2011

In this WP the **Surface plasmon polariton absorption modulator (SPPAM)** will be fabricated on a SOI chip. The SOI chip containing silicon waveguides will be used for postprocessing to produce the four-layer structure close by the silicon wire waveguide. In spite of, the relatively small dimensions of the SPPAM we believe that we have all the expertise and facilities for its fabrication. Making use of optimized geometrical and material properties obtained from Task 3.2, the device will be fabricated following to the corresponding fabrication steps.

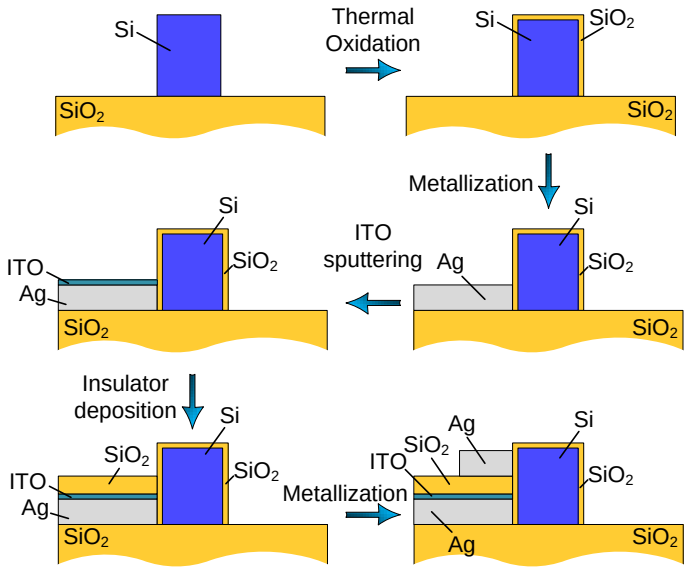


Figure 1.3.4 Silicon wire waveguide fabricate on a SOI chip with conventional CMOS technology. Very thin oxide layer will be produced via thermal oxidation around the silicon wire waveguide. Contact lithography followed by metallization will be employed for structuring the bottom electrode. ITO will be produced on the top of the electrode via RF magnetron sputtering. The insulator layer will be evaporated on the top of the silver layer. The properties of the entire plasmonic waveguide will be defined by defining the width of top metal patch.

The second modulator approach in NAVOLCHI aims to exploit the combination of both electrical and optical field enhancement in the plasmonic nano-structures containing highly nonlinear organic polymers to reduce the dimensions of conventional Pockel's effect based Mach-Zehnder Modulators (MZM). Plasmonic nano-slot waveguides show extraordinary optical field confinement in the insulator gap sandwiched between two metal electrodes. Filling the gap between metal patches with highly nonlinear organic polymers activates initially passive plasmonic nano-slot waveguides for their application as phase modulators. It has been reported that complete on/off in the plasmonic MZM can be achieved in the device length shorter than 1μm[49]. However, the reported device operates at wavelength of 800nm, which enhances the nonlinear interaction even further due to the plasmonic energy density enhancement at the metal/polymer interface.

NAVOLCHI will design plasmonic nano-slot based ultra-compact MZM modulators for low voltage optical modulation at the telecommunication wavelength of $1.55\mu m$. First simulation data shows the feasibility of this approach for achieving accumulated phase shift of π in the device length of $20\text{-}40\mu m$ with the overall 12-23dB plasmonic losses.

Technical description of the implementation of innovations from WP4, Plasmonic Receiver

The plasmonic receiver consists of two main parts, a plasmonic pre-amplifier and a photo-detector.

For the **pre-amplifier**, we propose to use colloidal quantum dots (such as PbS, PbSe and more advanced) for providing gain. These quantum dots are fabricated in solution using chemical methods and

[49] S.-I. Inoue and S. Yokoyama, Numerical simulation of ultra-compact electro-optic modulator based on nanoscale plasmon metal gap waveguides, Electronics Letters **45**, 1087–1089 (2009).

potentially provide a cheap alternative for more traditional III-V epitaxial materials. Recently, several groups demonstrated gain [50] using such quantum dots. However, in most cases the gain was limited by lack of optical confinement in the active layer. In this project, we will study two plasmonic structures, which overcome this problem by concentrating the light in the active layer. There are two possible schemes can be contemplated for the waveguide design as described below.

One-Dimensional (1D) metallic waveguide with combination of gain medium

The main concept of the first device is similar to the one proposed in [51], where a thin gold layer is embedded in a polymer partially doped with a dye (1 μm above the gold layer). This provides gain into the plasmon guided modes when the polymer is pumped optically. We propose the use of a polymer doped with PbSe quantum dots (QDs) that can furnish optical gains around 100 cm^{-1} [51]. In these conditions, if the plasmon frequency equal to that of the ground state absorption/emission in quantum dots (at target wavelengths of 1.31-1.55 μm), a resonance between the plasmon and QDs is expected, and gain to the light propagated by the plasmon could be obtained. Alternatively, an external source for optical injection (let say 980 nm, for example) can be defined to produce photons at the SPP wavelength that is resonant with the QD ground state.

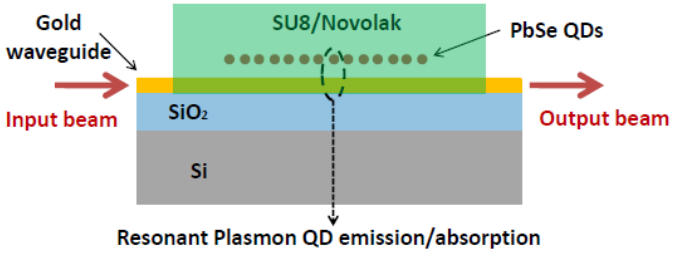


Figure 1.3.5 1D SPP waveguide covered with a gain media based on PbSe QDs embedded into UV patternable resists.

The proposed design is depicted in Figure 1.3.5 as the simplest situation: a SPP is guided in a quasi-1D waveguide and a gain medium is cladding it. The cladding can be designed to guide light emitted by QDs (a dielectric stripe). Even if this will increase the final footprint of the amplifier, this cladding can be thought as light coupler to external optical fibers and encapsulation at the same time and/or used to produce gain for several plasmonic waveguides (several channels) at the same time.

Hybrid silicon-plasmonic structure

[50] R.D. Schaller M. A. Petruska, and V. I. Klimov, Tunable Near-Infrared Optical Gain and Amplified Spontaneous Emission Using PbSe Nanocrystals, J. Phys. Chem. B, 107, 13765 (2003).

[51] R.D. Schaller M. A. Petruska, and V. I. Klimov, Tunable Near-Infrared Optical Gain and Amplified Spontaneous Emission Using PbSe Nanocrystals, J. Phys. Chem. B, 107, 13765 (2003).

The second plasmonic waveguide structure is based on a silicon based hybrid plasmonic waveguide which is recently been proposed by Dai *et al.*, [52]. The structure is shown in Figure 1.3.6 below. It consists of a standard silicon waveguide with a thin oxide layer and a metal layer on top. Due to a combination of slot waveguide effects and plasmonic effects, the light is very strongly confined in the oxide layer. Moreover, by controlling the width of the waveguide, the confinement vs. propagation length trade-off can be controlled easily and coupling to a standard silicon waveguide with good efficiency is possible.

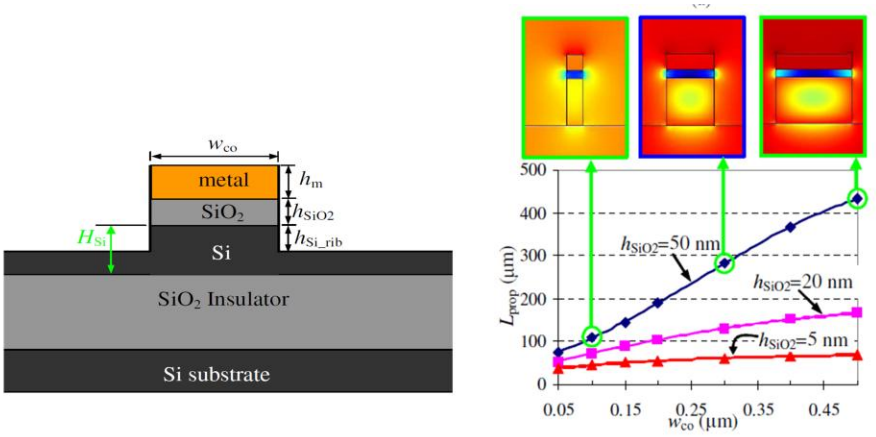


Figure 1.3.6 Hybrid silicon-plasmonic waveguide showing basic structure (left) and propogation length vs. confinement trade-off [58].

We propose to include the quantum dots active layer in the thin oxide layer to achieve confinement of >50%. In addition, this structure is well adapted to the electrical injection also. We will design the structure for the optimal gain with a suitable figure of merit (confinement vs. losses) while optimizing the coupling to a standard waveguide.

As discussed earlier, the amplification in IV-VI quantum dot based devices suffer from high Auger recombination, which limits the gain and oxidation, and thus limits the long term reliability. Therefore, we are optimizing the basic IV-VI QDots towards higher gain and long term stability. Both aspects can be improved by growing multilayer QDots (e.g. PbS/PbSe core-shell particles) and controlling their shape (e.g. giant particles or rod-type particles), which will be studied experimentally to analyze the performance of the plasmonic amplifiers.

In addition, for practical applications, an efficient electrical injection scheme is required. Currently, organic semiconducting layers are being used to realize electrically injected LED's based on QDots. However, the maximum current density allowed in these layers is limited. Therefore, we will pursue an alternative approach, which would be based on work recently carried out by Caruge et.al. [53]. They demonstrated current injection through semiconducting oxide layers in combination with CdSe QDs emitting in the visible using the basic device depicted in Figure 1.3.7. These injection layers allow for

[52] D. X. Dai and S. L. He, "Low-loss hybrid plasmonic waveguide with double low-index nano-slots," *Optics Express*, vol. 18, pp. 17958-17966, Aug 2010.

[53] J. M. Caruge, *et al.*, "Colloidal quantum-dot light-emitting diodes with metal-oxide charge transport layers," *Nat Photon*, vol. 2, pp. 247-250, 2008.

several orders of magnitude larger current density. We will investigate the transfer of this technology to the IR-region, and its incorporation in the hybrid silicon-plasmon waveguide structure introduced above.

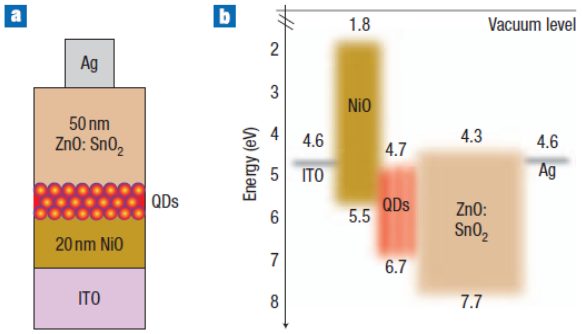


Figure 1.3.7 Electrically injected quantum dot based LED using inorganic semiconducting injection layers [[53]].

The second receiver component developed in NAVOLCHI is the **plasmonic photodetector**, which should be able to measure SPP signal coming from different plasmonic waveguide channels on the same chip or another connected chip to convert plasmons into photons into an electrical signal. Alternatively, using plasmonic approaches, the responsivity of the photodetector can be increased dramatically, however at the cost of reduced final footprint of the final device. Both concepts can make use of colloidal QDs eventually embedded into conductive polymers to define micrometric photodetection on Si substrates[54] or directly into nanogaps between metal contacts (plasmon effects can be also a design parameter) [[55]], [[56]]. Both concepts are illustrated in Figure 1.3.8. In both cases, QDs absorb light and photogenerated carriers are transferred contributing to the increase of the conductivity. In the second case (right side panel), metal (Au, Ag) nanorods are dispersed in the conducting polymer enhancing light absorption at a wavelength resonant with the longitudinal localized surface plasmon (of the nano-rod).

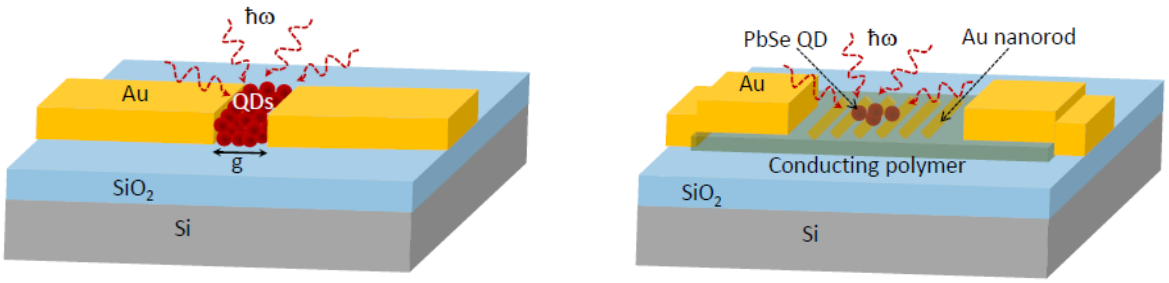


Figure 1.3.8 (left) Metal nanogap photoconductor containing QDs between electrodes with an effective absorption edge $\lambda_g > 1.6$ μm; (right) Photoconductor containing similar QDs plus metal nano-rods whose length would resonantly couple light at telecom wavelengths.

[54] T.P. Osedach,_ S.M. Geyer, J.C. Ho, A. C. Arango, M.G. Bawendi, and V. Bulovic, Lateral heterojunction photodetector consisting of molecular organic and colloidal quantum dot thin films, Appl. Phys. Lett. **94**, 043307 (2009).

[55] Willis, L.J.*, Fairfield, J.A., Dadosh, T., Fischbein, M.D., and Drndic, M. (2009). Controlling nanogap quantum dot photoconductivity through optoelectronic trap manipulation. Nano Letters, 9 (12), 4191-4197.

[56] M.C. Hegg, M.P. Horning, T. Baehr-Jones, M. Hochberg, and L.Y. Lin, Nanogap quantum dot photodetectors with high sensitivity and bandwidth, Applied Physics Letters, 96: 101118 (2010).

Photon-Plasmon coupling

To couple plasmon-photon to the photoconductive material, a 1D metallic waveguide can be made by ebeam lithography and metal deposition (some proof of concept will be undertaken by using crystalline nanowires manipulated with AFM) on top of a polymer nanocomposite photodetector.

The photoconductive material can be prepared in a solution of the conducting polymer containing small nanowires of appropriate dimensions to have longitudinal Localized Surface Plasmon Resonance (LSPR) mode at around 1.55 μm. In this way the light coupling from another off-chip or on.chip component can support only free space or organic based waveguides (SU8, Novolak). A temperature change induced in the polymer by the SPP losses or LSPR can lead to conductivity changes in the conductive polymer (polythiophene family), given its typical high sensitivity of electrical and optical properties to temperature (dependent also on preparation conditions)[57]. The dimensions of the planar polymer photodetector can be limited by using a bi-polymer composite in which one of them has lithographic properties like Novolak, as illustrated in Figure 1.3.9). These polymers can exhibit conductivity in a broad range (up to 200 S/cm^2 in our developments) and UV lithography patterning is possible, as shown in the bottom panel in Figure 1.3.9. Furthermore, the metal nanoparticles can be synthesized in situ (see Transmission Electron Microscopy image at the bottom-right of Figure 1.3.9). In this project we will firstly demonstrate the capabilities of these plasmonic-conductive polymers to detect light through plasmon interaction.

QDs and conductive polymers

QDs can be incorporated as sensitizers in the above described polymer nanocomposite (lithographic and conductive) or simply deposited as a layer on top of the polymer layer. In this way photons transformed from plasmons during propagation (or direct incident light) can be absorbed by QDs and photogenerated excitons lead to conductivity changes after electric field dissociation. This simple idea was depicted in Figure 1.3.8 (left) of Section 4.2, the nanogap photodetector in which a PbSe QD layer was deposited into that nanogap between the metal electrodes. Alternatively, the QD layer can be deposited on top of the plasmonic polymer structure explained before (or dispersed in the polymer before deposition by spin-coating), as was illustrated in Figure 1.3.8 (right). Characterization by confocal microscopy and SNOM will be developed to illuminate small footprint photoconductors.

[57] A. B. Kaiser, Systematic Conductivity Behavior in Conducting Polymers: Effects of Heterogeneous Disorder, Adv. Mat. 13, 927–941, (2001).

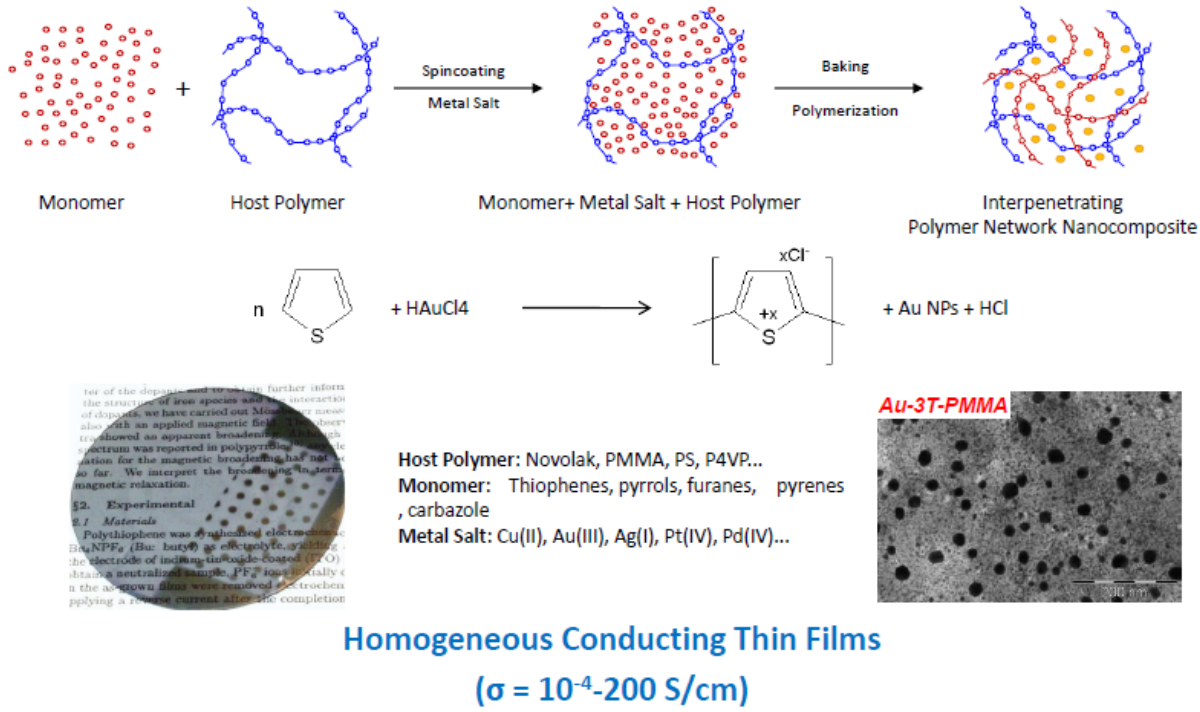


Figure 1.3.9 Conducting polymers produced in the matrix of a photolithographic resist plus the (optional) simultaneous synthesis of metal nanoparticles (to be published).

Technical description of the implementation of innovations from WP5, Plasmonic Optical and Electronic Intefaces

Next to the advanced active plasmonic devices being developed in WP3 and WP4, we would need several supporting passive components, such as silicon to plasmonic waveguide couplers, chip-to-chip couplers and optical noise filters. Moreover a set of CMOS circuits are required in order to allow electronics to interact properly with the plasmonic interconnects layer. All of these components are designed and fabricated in WP5, which are described as follows:

Si waveguide to plasmonic waveguide coupler

Plasmonic devices are considered to be indivisible parts of the future large scale integrated photonic circuits due to their possible ultra-compact size and ultrafast performance. However, photonic low loss passive components such as simple waveguides which are able to transfer a signal in a distance of several centimetres with negligible loss still remain the best solution for on-chip communication. Therefore, couplers between these two technologies are desirable. **NAVOLCHI** will model efficient plasmonic couplers for light coupling into the plasmonic metal-insulator-metal (MIM) waveguides for the modulator and into the hybrid silicon-plasmonic waveguides for the amplifier. Because of the strong-field confinement at plasmonic structures, the coupling efficiency strongly depends on both material and geometrical properties of the coupler and the plasmonic structures. Using powerful electromagnetic simulation tools several types of silicon to plasmonic waveguide couplers will be optimized. The figure below gives an example of a coupler between a silicon waveguide and a plasmonic MIM waveguide.

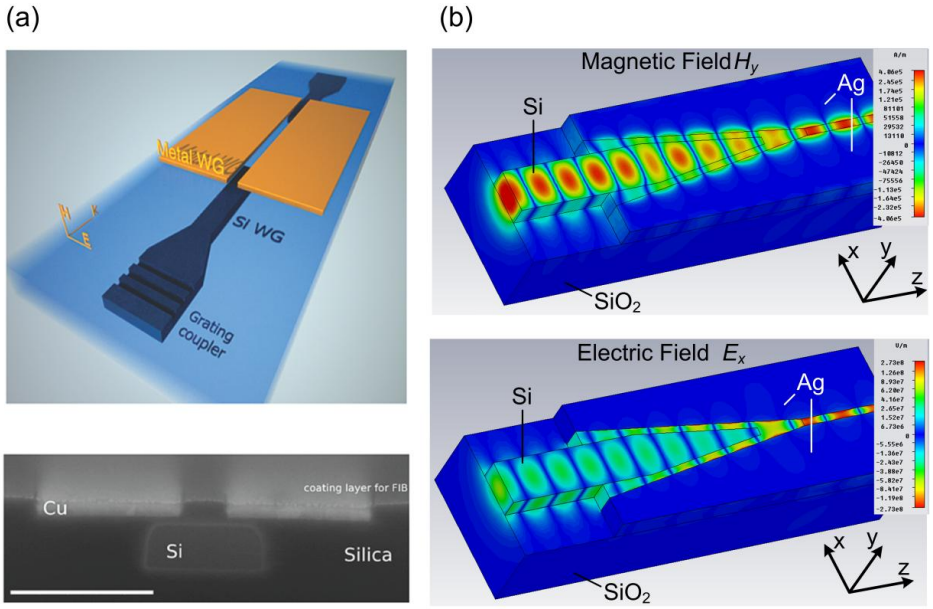


Figure 1.3.10 Examples for directional and tapered metallic couplers are represented. (a) Vertical directional coupler between silicon wire and copper-silica-copper plasmonic slot (100nm) waveguides [58]. The light is coupled vertically into the plasmonic slot waveguide via direction coupler with the length of the half of beat length. (b) The magnetic and electric field distribution in the tapered metallic couplers. The photonic mode from silicon waveguide is funnelled into the plasmonic nano-slot waveguide.

Si beam shaper

The goal of NAVOLCHI is to develop a solution for interconnecting multiple chips within a MCM-package. Hence, the optical signal has to be coupled between different chips. The standard edge coupling approaches are not practical due to fabrication and integration complexity (i.e. no access to edge of chip in standard CMOS flows). Therefore, the surface coupling method is considered by using surface grating couplers for coupling light from a highly confined sub-micrometer silicon waveguide to standard single mode fibers. This coupling approach has been extensively investigated in literature (in particular by consortium partner IMEC). And, it is now well understood how to perform this coupling with <1.5dB loss and good alignment accuracy. However, within NAVOLCHI we want to couple light between different chips in the package. Therefore, we need to be able to shape the form of the beam and focus it at larger distances (order millimeter). We will consider two approaches for realizing such beam shaping:

Directly designing the actual grating in such a way that it generates a focused spot. This has been demonstrated in the past using weak gratings. It is more difficult using the strong gratings typically used in silicon photonics. The goal of the design effort is to define the best compromise between size of the grating, attainable focal distance and bandwidth of the grating.

[58] Cecile Delacour, Sylvain Blaize, Philippe Grosse, Jean Marc Fedeli, Aure´lien Bruyant, Rafael Salas-Montiel, Gilles Lerondel, and Alexei Chelnokov. "Efficient directional coupling between silicon and copper plasmonic nanoslot waveguides: toward metal-oxide-silicon nanophotonics". *Nano Letters*, 10(8):2922–2926, 2010.

Introducing a diffractive element between both chips that focuses the beam. The diffractive element will be defined using sub-wavelength gratings in a thin silicon layer. Compared to classical micro-optical elements these might have big advantages in fabrication and assembly cost. Such diffractive gratings have been extensively studies within IMEC [59] and recently also other groups have used them for similar purposes [60]. The diffractive element may be introduced either between both chips to be coupled (working in transmission) or at the backside of one of both chips (working in reflection). The latter case allows additional freedom in design.

Ultra-compact optical noise filters

To enhance the responsivity of the receiver, we introduced an optical amplifier in the system (see WP4). This however requires optical filtering of the signal to suppress noise before the detector. Therefore, we will design compact optical filters with the target specifications of bandwidth of 2 -3nm, loss <2dB, nose suppression ratio >10dB, and free spectral range of >30nm. We will fabricate the filter by following these two approaches as below:

Fully passive optical filter by using passive silicon circuits. IMEC had recently showed very high quality ring and disk resonators [61] to serve as the basis for realizing this filter.

As an alternative, we will design and fabricate relatively more compact filter solution with the possibility of incorporating the filter directly into the plasmonic amplifier. This will be achieved by using a low Q-cavity around the amplifier or in the last part of the amplifier. The trade off between noise-suppression, filter quality and size will be studied in detail.

Signal Generation Module design [ST]

A main objective of this task is to implement on-chip electronics to be interfaced with the plasmonic devices in order to build the chip to chip interconnects. The target electronic device, called Dual Die Communication Module (DDCM), will follow a layered approach of the ISO-OSI standard. And, this will be responsible for the implementation of all the layers except the physical layer, represented by the plasmonic devices. Such blocks will be encoded using VHDL as hardware description language, will be synthesized using CMOS technology libraries and characterized in terms of area occupancy, timing (i.e. speed) and power consumption.

As shown in Figure 1.3.11 the DDCM top level in each die consists of a transmitter (DDCM Tx) and a receiver (DDCM Rx). In such a figure it's possible to see the two information flows supported by a complete DDCM architecture, i.e.

[59] R. Baets, B. Demeulenaere, B. Dhoedt, S. Goeman, "Optical system with a dielectric subwavelength struture having a high refractivity and polarization selectivity", patent EP-0798574 (Granted, 4/1997), US patent US-6191890 B1 (Granted, 2/2001)

[60] D. Fattal, J. Li, Z. Peng, M. Fiorentino, and R.G. Beausoleil, "Flat dielectric grating reflectors with focusing abilities," Nature Photonics, vol. 4, 2010.

[61] Results accepted for presentation at OFC 2011

Requests from initiators in chip 1 to targets in chip 2, responses from targets in chip 2 to initiators in chip 1, virtual wires from chip 1 to chip 2 (continuous lines);

Requests from initiators in chip 2 to targets in chip 1, responses from targets in chip 1 to initiators in chip 2, virtual wires from chip 2 to chip 1 (dotted lines).

The DDCM transmitter (DDCM Tx) is responsible for

Receiving requests from initiators in the same die and sending them to targets in the other die

Receiving responses from targets in the same die and sending them to initiators in the other die

Sampling ancillary signals (virtual wires) generated in the same die at a specified rate and sending samples to the other die

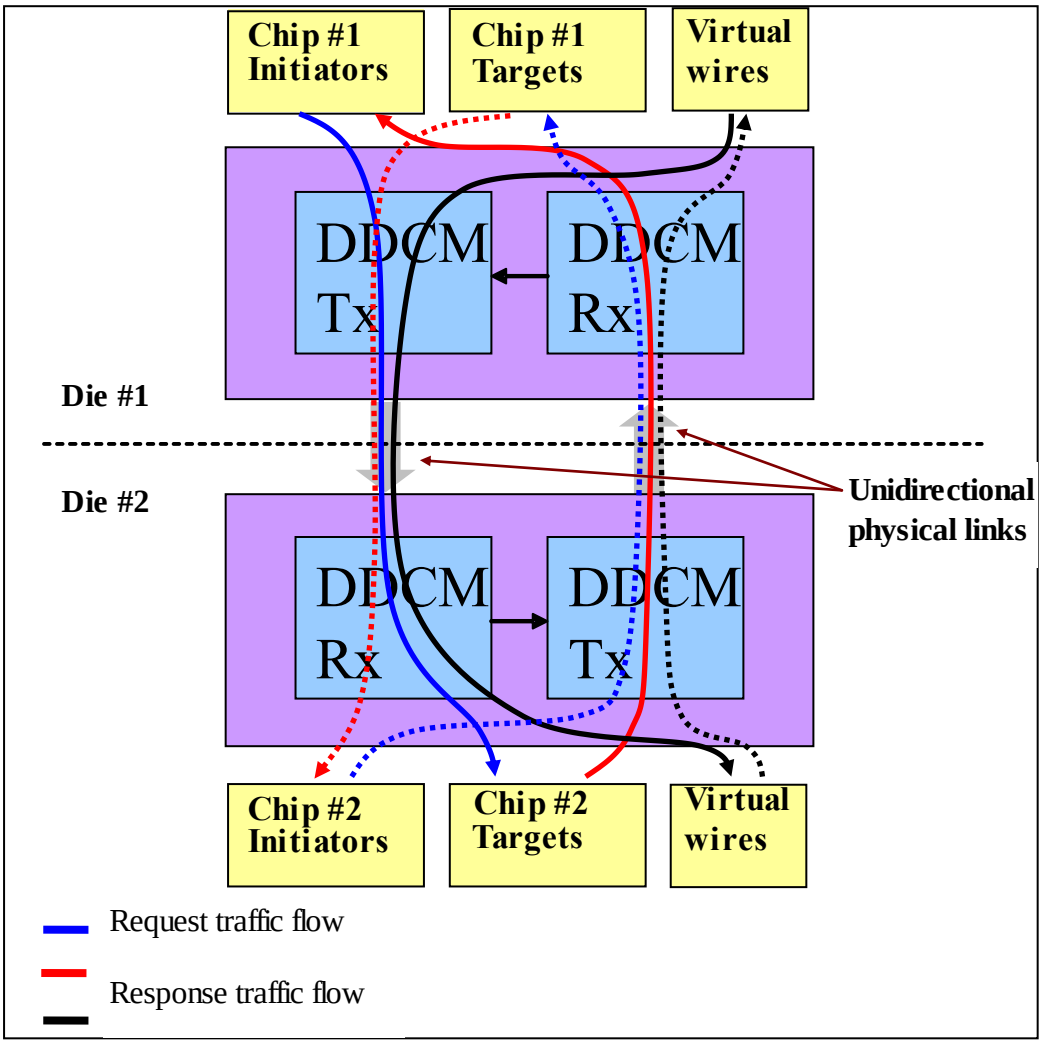


Figure 1.3.11 DDCM top level architecture and information flow

The DDCM receiver (DDCM Rx) is responsible for

Receiving requests from initiators in the other die and sending them to targets in the same die

Receiving responses from targets in the other die and sending them to initiators in the same die

Receiving ancillary signals samples generated in the other die and sending them to the proper destination in the same die Tasks 5.5: Signal Generation Module implementation via FPGA [ST]

In this task ST will exploit FPGA technology to implement as real hardware the DDCM block designed within task 5.4 so that if no technological issues and limitations will be highlighted, the configured FPGA can be used together with the plasmonic interconnect prototype for physical characterization and validation.

Technical description of the implementation of innovations from WP6, Integration, Characterization and Testing

The main objective of this Work Package is the characterization of all active and passive chips, the assembly, and packaging of all parts up to the packaging into a system-in-package (SiP).

Last but not least the SiP will be characterized, real data streams generated from FPGAs with code adapted to the system will be used to test and characterize the device an benchmark it against state-of-the art solutions.

The system-in-package packaging is a challenge. KIT will use its LIGA technology (Lithography, Galvanisation and Molding) to fabricate ultra-precise alignment modules for an alignment of the chips with 1 µm tolerance. This will allow for system-in-package (SiP) assembly by means of beam shapers. The technique for packaging has been tested previously (in a different but similar form) by the project MISTRAL, funded by the German Ministry of Science.

B1.3.1.3. Significant risks and associated contingency plans

Having in mind that some risks may have an impact on the project schedule and project objectives and finally may lead to contractual issues, the management process shall identify and monitor internal and external risks for the project and take appropriate measures.

Internal risks can stem from:

The technical nature of the R&D: unexpected technical difficulty, key technologies not available,

Problems with a partner: partner under performing or key partner leaving the project,

Project execution risks: key milestones or critical deliverable delayed,

Poor communication and cooperation between the partners,

External risks are essentially coming from the existence of other industrial solutions as well as from worldwide competing R&D efforts.

Mitigation is undertaken at the appropriate level in the project organisation: work-packages, Project Management Committee or General Assembly in accordance with the rules defined in the Consortium Agreement.

Some of the major risks concerning the implementation of the objectives have been already considered in the proposal preparation phase and specific contingency actions/plans have been specified. In that respect:

(1) Partners with some overlapping expertise have been invited to the consortium, and although that they work on complementary tasks, they do have the know-how to cover topics assigned to other partners.

(2) Some activities on objectives that promise to deliver components with extremely good performance but have been considered of higher risks are complemented by alternative lower risk component development activities.

The following table summarizes the main identified risks within the NAVOLCHI project, the impact that these would have to the project completion and the appropriate actions that should takes as a contingency plan.

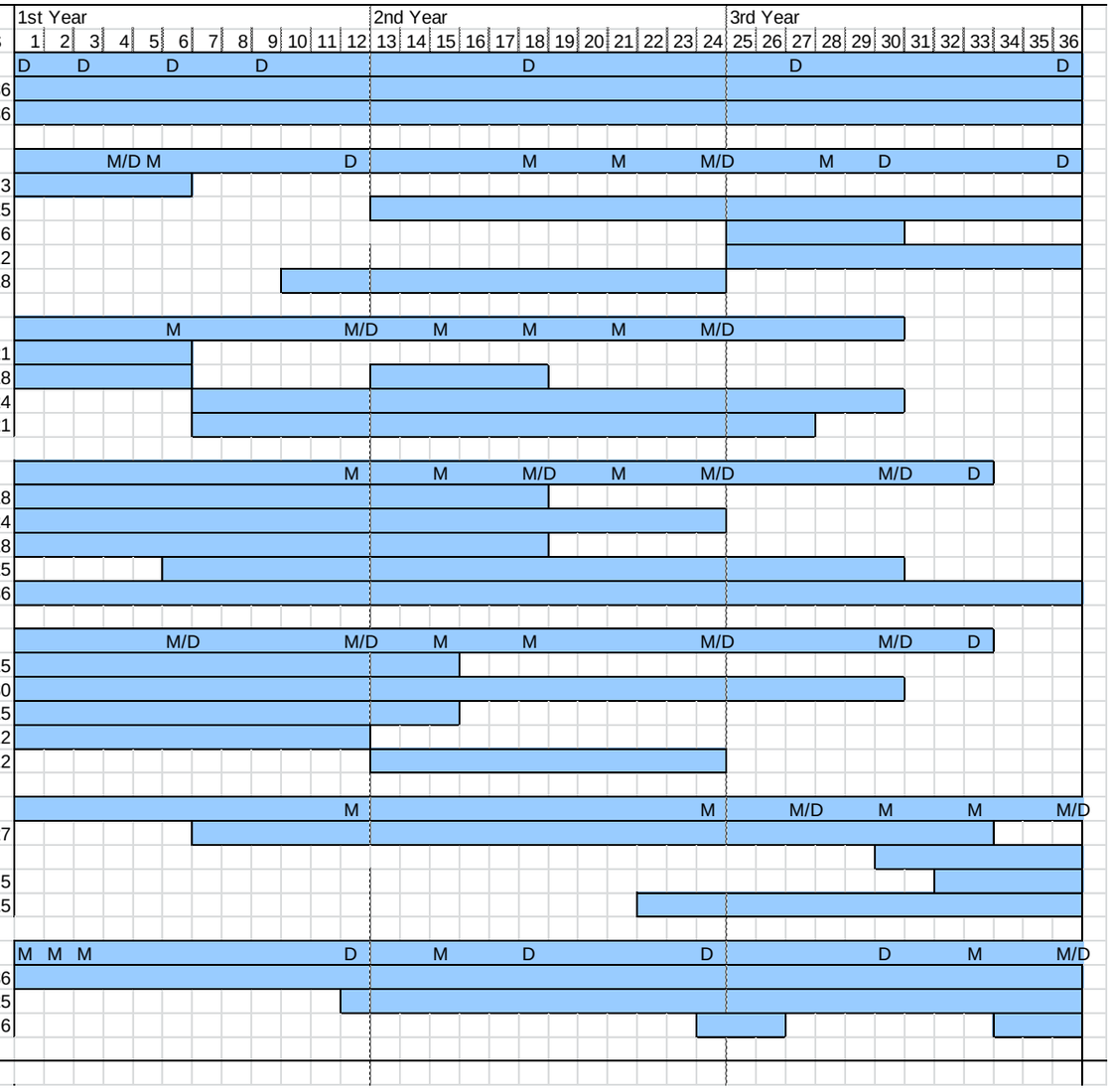
Risk Identified	**Impact**	**Contingency Plan**
Plasmonic laser output is weak	Objectives 1a	A plasmonic amplifier may solve this issue. Alternatively, we have foreseen high-sensitivity photodiodes and may even use avalanche photodiode concepts
The extinction ratio of the ultrafast plasmonic modulator is not good enough.	Objectives 1b	Direct modulation of the plasmonic laser may then be used instead. We expect the direct modulation speed to be slower - yet, 10 Gbit/s still will be possible.
Overall plasmonic losses are too high and as a consequence sensitivity is low and speed is low as well	Objective 4	Each of the plasmonic structures might be higher loss than anticipated. So the strategy is to introduce with highest priority low loss plasmonic structures as outlined in literature. Second, there is a replacement for each and every component that might be used instead. The modulator might be replaced by a direct laser modulation scheme, the amplifier and photodetector might be replaced by APD the free space beam focusing technique might be replaced by a standard fiber connection.
Plasmonic amplifier does not provide sufficient gain	Objective 2a	A larger output power plasmonic laser might be used instead or the plasmonic PD might be replaced by an APD.
The plasmonic photodetector does not work.	Objective 3 can not be met	In that case, IMEC will build a back-up detector consisting of a commercial avalanche detector, integrated on a silicon photonics circuit using conventional flip-chipping

		techniques, as is schematically shown in the figure below. This task involves selection of the most optimal avalanche detector, design of the coupling structure (either using grating coupler for surface type detector as shown in the picture or using inverted taper for edge type detector - not shown), and flip-chipping of detector on the platform. Based on past experience a coupling efficiency better than 3dB is expected.
Free space interconnection scheme fails	Objective 3b	A fiber coupling scheme might be used instead.
A key partner leaves the project	WP 3, 4 and 5 would be at risk	All partners bring in key expertise to the project and have committed with an emphasis on one WP. Yet, also all partners have additional expertise in related technologies. Plasmonic laser: TUE is committed to this – but IMEC has experience in the field as well and could replace TUE Plasmonic modulator: KIT is committed to this task. UV has related activities and could replace KIT. Plasmonic Detector: UV is committed to this task. KIT could replace UV Silicon Photonic fabrication: IMEC has fully committed to this work. TUE and KIT have similar technologies, yet not with photolithography but E-Beam lithography. The yield would be worse then – but not the outcome of the result.
Underperforming partners; Poor communication and cooperation between the partners;	Key milestones or critical deliverable delayed	Very dense project management structure with an experienced group as coordinator. The management structure is set out such that the Project Coordination Committee in accordance with the rules defined in the Consortium Agreement can take immediate actions to improve operations and penalize the responsible partners

B1.3.2. *Timing of work packages and their components*

This section shows a Gantt chart with the timing across all WPs and tasks. The milestones and deliverables are included as well.

		Start	End	S
WP1	**Project Management**	**1**	**36**	
	1.1: Project Organization and Management	1	36	36
	1.2: Project Quality Management	1	36	36
WP2	**Definition and speci-fications of plas-monic chip-to-chip interconnection plat-form**	**1**	**36**	
	2.1 Analysis of chip to chip interconnect requirements and needs	1	3	3
	2.2 Modeling of devices and system for communications applications	12	36	25
	2.3 Value analysis in terms of cost and green aspects	25	30	6
	2.4 Techno-economical evaluation and benchmarking	25	36	12
	2.5 VHDL modelling of plasmonic interconnect and CMOS interface circuits	10	27	18
WP3	**Plasmonic Trasnmitter**	**1**	**30**	
	3.1 Modelling of device structures plasmonic laser and optimization of bonding technology	1	12	21
	3.2 Modelling of plasmonic modulator	1	18	18
	3.3 Fabrication of nano plasmonic laser	7	30	24
	3.4 Fabrication and characterization of Si-plasmonic modulators	7	27	21
WP4	**Plasmonic Receiver**	**1**	**36**	
	4.1 Design and modelling of plasmonic pre-amplifier for receiver	1	18	18
	4.2 Modelling of plasmonic QD polymer based photodetectors	1	24	24
	4.3 Colloidal quantum dots with optimized gain and electrical injection scheme	1	18	18
	4.4 Fabrication and characterization of QD-based plasmonic amplifiers	6	30	25
	4.5 Fabrication and characterization of plasmonic polymer QD based photodectors	1	36	36
WP5	**Optical and electrical interfaces for plasmonic interconnection platform**	**1**	**30**	
	5.1 Modelling and fabrication of coupling Si waveguide to plasmonic waveguide	1	15	15
	5.2 Modeling and fabrication of Si beam shaper	1	30	30
	5.3 Modeling and fabrication of passive ultra-compact components as filters	1	15	15
	5.4 Singal generation module implementation	1	12	12
	5.5 Signal Generation Module implementation via FPGA	13	24	12
WP6	**Integration, characterization and testing**	**7**	**36**	
	6.1 Characterisation of active and passive plasmonic devices	7	33	27
	6.2 Assembly and packaging of plasmonic devices into System-in-Package	30	36	
	6.3 Plasmonic chip to chip interconnect prototype testing and evaluation	32	36	5
	6.4 System-in-Package integration and characterization	22	36	15
WP7	**Dissemination and Exploitation**	**1**	**36**	
	6.1 Dissemination of results	1	36	36
	6.2 Exploitation of results	12	36	25
	6.3 Promotion of Results	24	36	6



B1.3.3. *Description of Work*

WP1 − Project Management

Description of work

The work package will be led by KIT. It is subdivided into several tasks:

Task 1.1 Project supervision, organisation and monitoring [M01 – M36]

This task is devoted to organization, securing and managing resource of the consortium to bring about the successful competition of goals and objectives covered by NAVOCLHI.

a) Strategic management at project level
b) Control of work package activities, including technical quality control
c) Organisation of project reporting and meetings
d) Control of deliverable preparation
e) Conflict management

Fed by: All WPs

Feeds: All WPs

Task Leader: KIT

Contributing partners: All

Task 1.2 Project Quality Management [M1 – M36]

This task specially devoted to the assessment of the quality of the work and the deliverables produced in the project. The objectives of this task are to ensure adequate quality of the outcomes of the project:

a) Quality of the produced deliverables
b) Quality of the internal deliveries

Fed by: All WPs

Feeds: All WPs

Task Leader: KIT and WP leaders

Contributing partners: All

WP2 − Definition and specifications of plasmonic chip-to-chip interconnection platform

Objectives

This work package will investigate the new plasmonic device technology for chip-to-chip interconnection. An important activity is the development of a cycle accurate VHDL functional model of the plasmonic interconnects for cosimulation with the digital part VHDL and FE netlist. During this phase the development of a cycle accurate functional model of the serializer and the deserializer representing the link between the on-chip electronics digital part and the plasmonic interconnect will be required as well. In particular, the main objectives are:

- To identify advanced interconnections functionalities targeted to chip-to-chip communication for the developed plasmonic integrated photonic components.
- To define optical interconnection system environment and parameters within which the plasmonic devices have to function and that will be used for evaluating its performance with respect to processor to processor communication in data centres.
- To investigate the optical interconnect system level specifications that should be met for each of the respective potential chip-to-chip communications. To develop a cycle accurate VHDL model of plasmonic interconnect
- To develop a cycle accurate VHDL model of serializer/deserializer
- To evaluate the efficiency of the proposed solutions in terms of cost and green aspects with respect to the existing technology solutions

Description of work

The work package will be led by AIT and is split in the following tasks:

Task 2.1 Analysis of chip to chip interconnect requirements and needs (bandwidth, latency, power consumption, noise immunity) [M1-M6]

The objective of this task is to analyze and understand requirements and needs, in terms of bandwidth, latency, power consumption and noise immunity, of chip to chip communication for systems split over more dice, implementing real applications (consumer, automotive, etc.). Such an analysis will lead to the specification of suitable architectures of the systems, a proper microarchitecture of a Die to Die Communication Module (DDCM) and an accurate characterization of the performance required for the physical layer (PHY). This last point, initially affecting the traditional electrical PHY used in a first phase, will be the key for the specification of the plasmonic interconnect in order to meet the chip to chip communication required performance.

Fed by: Prior know how of involved partners

Feeds: WP2 - Task 2.2, 2.3

Task leader: ST

Contributing Partners: AIT

Partner Contributions:

- ST will carry out the investigation relying on inputs from their product divisions according to the requirements of the products they will be working at
- AIT will examine the extracted chip-to-chip interconnect requirements and needs leading to the initial definition of plasmonic devices and material properties for chip-to-chip interconnection (M2.2) that will provide feedback to the modelling and device studies in task2.2

Task 2.2 Modelling of devices and system for communications applications [M13 – M36]

The aim of this task is to give device specifications for the novel disruptive plasmonic Si-photonic devices and its application in the chip-to-chip interconnection environment.

a) Define the plasmonic device specifications of laser, modulators, photodetectors, waveguide amplifiers, grating couplers
b) To define the chip-to-chip intercommunication system in terms of data rate, low cost and power consumption.
c) Define the optical interconnects specifications utilizing plasmonic devices parameters
d) To define a device and system reference scenario that will be used for the performance evaluation of the developed components with respect to chip-to-chip interconnections.

Initial plasmonic device design requirement and specifications will be issued in D2.2 on M12, wheras the full Investigation of chip-to-chip interconnection-level specifications employing input from the new plasmonic devices will be reported in D2.3 on M24. The last 12 month duration of the task will investigate new applications and opportunities and provide any additional updates utilizing the developed models.

Fed by: Prior know how of involved partners

Feeds: WP2, WP3, WP4, WP5

Task leader: AIT

Contributing Partners: AIT, ST, KIT, TUE, IMEC, UVEG

Partner Contributions:

- AIT will contribute to the investigation of the definition of plasmonic devices and optical interconnect system environment that will be used for performance evaluation studies of the developed technologies.
- KIT will contribute by giving input from device design and experiments on plasmonic modulator, optical amplifiers and passive components.
- TUE will explore new plasmonic laser design possibilities and configurations for hybrid integration with SOI waveguide.
- IMEC will provide a study on bonding methods, steering waveguide design, QD polymer based optical amplifiers.

- UVEG will provide a study on QD based plasmonic photodetectors and polymer based optical amplifiers
- ST will provide input on chip-to-chip optical interconnect system scenarios.

Task 2.3 Value analysis in terms of cost and green aspects [M25 – M30]

This task aims to evaluate the performance of the developed plasmonic devices and chip-to-chip interconnection platform with respect to the physical layer specifications that should be met within the proposed system scenarios from Task 2.1.

a) To define the applications for chip-to-chip intercommunication in terms of high data rate, low cost and power consumption.
b) Define the plasmonic PICs system requirement and specifications for data centres

Fed by: WP2 - Task 2.1, 2.2, WP3, WP4, WP5, WP6

Feeds: WP2 - Task2.4, WP3, WP4, WP5, WP6

Task leader: AIT

Contributing Partners: AIT, ST, KIT, TUE, IMEC, UVEG

Partner Contributions:

- AIT will perform simulation studies of plasmonic chip-to-chip interconnection environment and will provide system level specification with the performance of the developed plasmonic devices.
- ST will contribute to providing information on chip-to-chip interconnect system application scenarios with the system functionality and its requirements.
- TUE will provide initial plasmonic hybrid Si laser structures specifications
- IMEC will provide initial specifications for the developed waveguide amplifier
- UVEG will provide photo-detector specifications
- KIT will provide initial specifications over plasmonic transmitter and passive elements

Task 2.4 Techno-economical evaluation and benchmarking [M24-M36]

This task has the objective of evaluate and quantify the benefits of splitting a system over more dice (System in Package) with respect to the more traditional approach consisting of having the system in a unique die (System on Chip).

Fed by: WP2.2

Feeds: WP2-Task 2.4, WP3-Task 3.1, WP4-Task 4.1, WP5-Task 5.1, WP6-Task 6.1-6.5

Task leader: AIT

Contributing Partners: AIT, ST, KIT, TUE, IMEC, UVEG

Partner Contributions:

- AIT will lead Task 2.4 and will perform studies for the calculation of the total cost and power

consumption of the chip-to-chip interconnection platform and will compare the results of existing solution in the framework of the proposed applications. It will also, explore the benefits of the developed technology in the current market.

- ST will contribute to identify the applicability of the developed technology components according to technology status, evaluate the potential of this technology for new product roadmaps and current market trends related to its own target-business.
- TUE will provide performance results of developed plasmonic hybrid Si laser
- IMEC will provide device components manufacturer input.
- UVEG will contribute by passing on information for photo-detection results
- KIT will contribute to this task by passing on information about modulators and passive components

Task 2.5 VHDL modelling of plasmonic interconnect and CMOS interface circuits [M10-M24]

The objective of this task is to model in VHDL both the plasmonic interconnect and the CMOS interface circuits (serializer/deserializer) for interfacing CMOS logic with the interconnect physical layer.

Fed by: WP 2 - Task 2.2, task 2.3

Feeds: WP5 - Task 5.4

Task leader: ST

Contributing Partners: ST

Partner Contributions:

- ST will develop an accurate VHDL behavioural model of the analog parts (serializer/deserializer) representing the interface with the plasmonic interconnects, in order to carry out cosimulation with digital parts.
- ST will develop an accurate VHDL behavioural model of the plasmonic interconnect for cosimulation with digital parts.

WP3 – Plasmonic Transmitter

Objectives

This work package will investigate via simulation various parameters and strategies for the plasmonic transmitter component of the project. This component consists primarily of a plasmonic laser and a plasmonic modulator, both connected to SOI Si waveguides. After simulation studies the plasmonic laser and modulator will be fabricated and delivered to other work packages. In particular the main

objectives are:

- Simulation studies to optimize laser size and structure to obtain maximum output power into either a plasmonic or conventional SOI waveguide
- Electrically pumped plasmonic/metallic nano-laser devices bonded onto an SOI wafer with light coupled into either a plasmonic or conventional SOI waveguide
- Performance targets for the laser are an active region area less than approximately one square micron, and optical output power coupled into the waveguide of at least approximately 100 microwatts with an attempt to achieve output powers up to one milliwatt
- For the modulator, more than 10dB extinction ratio in the device length shorter than 10 μm will be demonstrated
- Modulation speeds up to 40Gbit/s and higher will be demonstrated.

Description of work

The work-package will be led by TUE and split in the following tasks

Task 3.1 Modelling of device structures plasmonic laser and optimization of bonding technology [M1-M6]

The aim of this task is to look at the choice of laser design and how to couple the laser output to the Si waveguide.

Fed by: WP 2- Task 1

Feeds: WP 3 - Task 3

Task leader: TUE

Contributing Partners: TUE, IMEC

Partner Contributions:

- TUE will explore new plasmonic laser design possibilities and configurations for hybrid integration with SOI waveguide. Some input from system specification will be used.
- IMEC will provide a study on bonding methods, steering waveguide design

Task 3.2 Modelling of plasmonic modulator [M1-M18]

The aim of this task is to look at the various designs for the modulator, simulate them and how they will couple to the Si waveguide. Finally to make a design choice that will be fabricated.

Fed by: WP2 - Tasks 2.2, WP5 - Task 5.1

Feeds: WP3 - Task 3.4

Task leader: KIT

Contributing Partners: KIT, IMEC

Partner Contributions:

- KIT will explore via simulation different plasmonic modulator designs suitable for integration with Si waveguides.
- IMEC will help with an information on the Si photonic technology and options for construction of the devices on the SOI wafer

Task 3.3 Fabrication of nano plasmonic laser [M7-M30]

In this task the actual nano laser will be fabricated. This process will consist of obtaining the epitaxial grown InP/InGaAs wafer, bonding it to the SOI waveguide structure, and then performing lithography, etch and material deposition steps to form the laser.

Fed by: WP6 - Task 6.1

Feeds: WP6 - Task 6.11

Task leader: TUE

Contributing Partners: TUE, IMEC,

Partner Contributions:

- TUE will fabricate the metallic nano-laser structures using their cleanroom facilities
- IMEC will fabricate and supply the Si waveguide and SOI wafer and perform the required bonding of the InP wafer to the SOI wafer

Task 3.4 Fabrication of Si-plasmonic modulators [M7-M27]

Here the actual modulator is fabricated. This will consist of bonding a structure to the SOI wafer, lithography then other processing steps.

Fed by: WP 3 Task 3.2

Feeds: WP6 - Task 6.10, WP6 - Task 6.12

Task leader: KIT

Contributing Partners: KIT, IMEC

Partner Contributions:

- KIT will fabricate the metallic Si-plasmonic modulators on a SOI chip.
- IMEC will fabricate and provide Si waveguide structures on a SOI wafer.

WP4 – Plasmonic Receiver

Objectives

The main objective is the development of Receiver technology through:

- Appropriate designs and modelling (Tasks 4.1 and 4.2)
- Development of plasmonic optical amplifier based on IV-VI colloidal nanocrystals (Tasks 4.3-4.4)
  - Optimum QDs and structures based on them to furnish maximum gain (Tasks 4.3)
  - Concepts developed to obtain gain from QDs by using optical injection (Tasks 4.4)
  - Gain from QDs by using electrical injection (Tasks 4.4)
- Development of Plasmonic photodetectors (Tasks 4.5)
  - Simple concept of QDs in metallic nano-gap photoconductors
  - Photodetectors based on Plasmonic Patternable Conductive Polymers (PPCP)

Description of work

The Work-package will be led by UVEG and split in the following tasks:

Task 4.1 Design and modelling of plasmonic pre-amplifier for receiver [M1-M18]

The aim of this task is the modelling of the device concepts to be designed for fabrication in Tasks 4.4. It is necessary to define the coupling between propagating SPP in the plasmonic waveguides (two types as described below) and the gain medium (optically or electrically excited). If data are not available in literature measurements will be necessary (contemplated in Tasks 4.3).

Main work:

a) SPP plasmonic waveguides: (a) 1D SPP waveguide on SiO_2 and polymer cladding (in section 1.3.2), (b) Si-on-SiO_2 based waveguide with a top metal stripe producing plasmonic confinement (Figure 1.3.5 in Section 1.3.2).
b) Gain medium based on IV-VI QDs producing photons (optically/electrically pumped) at 1550 nm. The density is a parameter limited by chemistry and geometry is defined by designs (Figure 1.3.5 and Figure 1.3.6 in section 1.3.2).

Fed by: UVEG and UGent (WP4 - Tasks 4.3)

Feeds: UVEG and IMEC (WP4 - Tasks 4.4) and all in WP5 - Task 5.6 (integration)

Task leader: AIT

Contributing Partners: KIT, UVEG, IMEC, UGent

Partner Contributions:

- AIT will contribute to the investigation of the plasmon propagation modelling in waveguides-(a)/ (b) without/with the presence of the gain medium in both devices.
- KIT will provide technical know support to AIT in modelling plasmonic waveguide amplifiers.
- UVEG will contribute by giving input parameters from device fabrication and experiments on waveguides-(a), gain medium based on IV-VI QDs and optical pumping.
- IMEC will contribute by giving input parameters from device fabrication and experiments on waveguides-(b) and optical/electrical pumping.
- UGent will contribute by giving input parameters from gain medium based on IV-VI QDs

Task 4.2 Modelling of plasmonic QD polymer based photodetectors [M1-M24]

The aim of this task is the simulation/modelling of the device concepts to be designed for fabrication in Task 4.5. We explore here (also for fabrication) several concepts that can be combined in a more complex device, after feedback from Tasks 4.5.

a) QDs on Si-SiO_2 substrates at the nanogap between metal nanocontacts (the nano-gap distance is a design parameter).
b) QDs on top of (or dispersed into) conductive polymers. The conductive polymers are synthesized in photolithographic resist matrices (in order to pattern micrometric structures). Preparation conditions determine conductivity of the spin-coated layers.
c) Metal nanoparticles created (or metal nano-rods dispersed into) conductive polymers. The conductive polymers are synthesized in photolithographic resist matrices (in order to pattern micrometric structures). Preparation conditions determine conductivity of the spin-coated layers. Thermal coefficient of the polymer is needed to model the influence of absorption of light resonant with the localized plasmons.

Fed by: UVEG and IMEC (WP4 - Task 4.5)

Feeds: All tasks in WP4 and WP6 in Task 6.1 - 6.2

Task leader: UVEG

Partner Contributions:

- UVEG will contribute to modelling and furnish input parameters from device fabrication and experiments on the different elements/devices (Tasks 4.3).
- KIT will participate in modelling of plasmonic photodetector.

Task 4.3 Colloidal quantum dots with optimized gain and electrical injection scheme [M1-M18]

The first objective of this task is obtaining basic information of different available IV-VI QDs (or nano-rods) to be explored here in respect to Auger recombination and oxidation effects. The second objective is the study of gain induced by dots in structures compatible with proposed device designs,

i.e., giving necessary data to develop Tasks 4.1 and hence for device fabrication (Tasks 4.4).

Main work:

a) Basic optical (including gain) and electrical properties of layers and layer stacks containing IV-VI QDs
b) Absorption/Gain measured in polymer thin films and stripes doped with IV-VI QDs

Fed by: Task 4.2

Feeds: WP4 - Tasks 4.1, 4.4 and WP5 - 5.1

Task leader: UVEG

Contributing Partners: UGent, UVEG

Partner Contributions:

- UGent will contribute in the synthesis of PbS, PbS/PbSe core-shell and rod-like nanoparticles, preparation of layers and in characterization (optical, electrical) of nanoparticles and layers..
- UVEG will contribute in the preparation of polymer-QD thin films and stripes (with UV-lithography) on Si-SiO_2 to study optical properties and gain during guided light propagation, as a function of geometry and QD density.

Task 4.4 Fabrication and characterization of QD-based plasmonic amplifiers [M6-M30]

The aim of this task is the fabrication and characterization of proposed designs (Figure 1.3.6 and Figure 1.3.7 in section 1.3.4.4) and appropriate feedback with Task 4.1 and 4.3.

a) Fabrication and characterization of 1D plasmonic waveguides (different types) on Si-SiO2
b) Absorption/Gain measured in polymer (and other dielectrics) thin films and stripes doped with IV-VI QDs
c) SPP propagation in plasmonic waveguides with QD doped polymer cladding layer
d) Fabrication and characterization of light propagation on metal(Au, Al, Cu)-Si on SOI waveguides
e) Gain layer stack in the metal-Si structure and test with optical and electrical injection

Fed by: AIT, KIT, UVEG, IMEC, UGent (WP4 - Tasks 4.1 and 4.3)

Feeds: All in WP6 – Task 6.1, 6.2 and 6.3

Task leader: IMEC

Contributing Partners: UVEG

Partner Contributions

- IMEC will contribute by fabrication of metal stripes on Si-SiO2 and on SOI based nano-waveguides. Measurements of propagation and losses.
- UGent will contribute on gain from QDs by optical and electrical pumping.

- UVEG will contribute by investigation of gain medium on a polymer matrix as a function of QD density. Fabrication of polymer-metal nanocomposites to achieve SPP waveguiding. Fabrication of polymer-QD claddings of metal nanowires (or metal stripes) on Si-SiO_2. Gain from QD composites by optical injection. Confocal and Near-field Optical experiments.

Task 4.5 Fabrication of plasmonic polymer QD based photodectors [M1-M36]

The aim of this task is the fabrication and characterization of proposed designs (Figure 1.3.8 in section 1.3.4.2) and appropriate feedback with Tasks 4.2.

a) Photoconductivity of IV-VI QDs in nanogaps defined between metal nanocontacts
b) Optimization of patternable conductive polymers (PCP) based on polythiophene in a Novolak matrix
c) Photo-conductivity at the localized surface plasmon resonance in plasmonic PCP (PPCP)
d) Photoconductivity of QDs dispersed/deposited in PPCP.

Fed by: UVEG, IMEC (WP4 - Tasks 4.2) and WP5 - Task 5.1(KIT), WP5 - Task 5.4(KIT, IMEC)

Feeds: All in WP6 - Task 6.3

Task leader: UVEG

Contributing Partners: IMEC, KIT

Partner Contributions:

- IMEC will contribute by fabrication of metal nanocontacts separated (nano-gap) in the range 20-80 nm on Si-SiO_2.
- UVEG will contribute in the fabrication and characterization (confocal/SNOM) of photodetectors based on QDs deposited on the nano-gap area of the device.
- UVEG will contribute in the development of photoconductors based on patternable conductive polymers, both directly due to plasmonic effects and due to charge transfer from QD sensitizers (dispersed in the polymer layer or deposited on top of it).
- KIT will intensively participate in the fabrication procedure of the plasmonic photodetector. Particularly, for full functionality of the plasmonic receiver, KIT will utilize the Si waveguide-plasmonic couplers developed in WP 5 in order to couple light from silicon waveguide into the plasmonic photodetector.

WP5 – Optical and electrical interfaces for plasmonic interconnection platform

Objectives

Next to the advanced active plasmonic devices being developed in WP3 and WP4 we need several supporting passive components, such as silicon to plasmonic waveguide couplers, chip-to-chip couplers and optical noise filters. All of these are designed and fabricated in WP5.

Moreover a Hardware (HW) module acting as interface between different chips (dice) is required; such a module is called Dual Die Communication Module (DDCM) and is also specified and designed within WP5. Such a module will support natively IP protocols from STMicroelectronics, i.e. STBus, VSTNoC and Spidergon STNoC.

In particular the objectives are:

- To design and simulate the couplers needed to efficiently couple light from the silicon backbone network to the highly confined plasmonic waveguide structures used for the laser, modulator and amplifier
- To design and simulate optically beam shaping gratings to direct light between chips separated by 1 mm
- To design and simulate compact filters to suppress noise originating from the optical pre-amplifier
- To fabricate these devices
- To specify, design and verify the Dual Die Communication Module.
- To implement the DDCM as a hardware module exploiting FPGA technology.

Description of work

The work-package will be led by IMEC and split in the following tasks:

Task 5.1 Modelling and fabrication of coupling Si waveguide to plasmonic waveguide [M1-M15]

Photonic low loss passive components such as simple waveguides which are able to transfer a signal in a distance of several centimetres with negligible loss still remain the best solution for on-chip communication. Therefore, couplers between these waveguides and the plasmonic devices developed in the project are needed. **NAVOLCHI** will model efficient plasmonic couplers for light coupling into the plasmonic metal-insulator-metal (MIM) waveguides for the modulator and into the plasmonic waveguides used for realizing the amplifier. Because of the strong-field confinement in the plasmonic structures, the coupling efficiency strongly depends on both material and geometrical properties of the coupler and the plasmonic structures. Using powerful electromagnetic simulation tools several types of

silicon to plasmonic waveguide couplers will be optimized.

Fed by: KIT (WP3 - Task 3.2) and IMEC, UVEG (WP4 - Task 4.1)

Feeds: KIT, UVEG and IMEC (WP5 - Task 5.4)

Task Leader: KIT

Contributing partners: IMEC, UVEG

Partner Contributions:

- KIT: Design of coupler to plasmon modulator
- IMEC: Design of coupler to plasmon amplifier
- IMEC: Fabrication of SOI backbone network, fabrication of gratings for beam shaping, fabrication of couplers, characterisation of devices
- UVEG: Design of coupler to plasmon amplifier
- KIT: Postprocessing for couplers to plasmonic modulators, characterisation

Task 5.2 Design and fabrication of Si beam shaper [M1-M30]

We want to design a scheme for coupling light between different chips in a package. Therefore we need to be able to shape the form of a beam coming from an SOI waveguide and focus it at larger distances (order millimeter). We will consider two approaches for realizing such beam shaping:

a) Directly designing the actual grating in such a way that it generates a focused spot. This has been demonstrated in the past using weak gratings. It is more difficult using the strong gratings typically used in silicon photonics. The goal of the design effort in this task is to define the best compromise between size of the grating, attainable focal distance and bandwidth of the grating.
b) Introducing a diffractive element between both chips which focuses the beam. The diffractive element will be defined using sub-wavelength gratings in a thin silicon layer. The diffractive element may be introduced either between both chips to be coupled (working in transmission) or at the backside of one of both chips (working in reflection). The latter case allows additional freedom in design.

Fed by: ST (Task 6.2 – system design, WP2)

Feeds: IMEC (WP5 - Task 5.4)

Task Leader: IMEC

Contributing partners:

Task 5.3 Design and fabrication of passive ultra-compact components as filters [M1-M15]

To enhance the responsivity of the receiver, we introduced an optical amplifier in the system. This however requires optical filtering of the signal before the detector. Therefore, in this task we will design compact optical filters, with specifications targeted for this function (2-3nm bandwidth, <2dB loss, >10dB suppression ratio, >30nm free spectral range. We will study two approaches:

Completely passive optical filter, using passive silicon circuits. IMEC recently showed very high quality ring and disk resonators, which can serve as the basis for realizing this filter.

As an alternative, possibly much more compact solution we will study the possibility for incorporating the filter directly into the plasmonic amplifier, e.g. by using a low Q-cavity around the amplifier or in the last part of the amplifier. The trade off between noise-suppression, filter quality and size will have to be studied in detail.

Fed by: ST, AIT (WP4 - Task 6.2 – system design), IMEC (WP4 - Task 4.1, WP4 - Task 4.4)

Feeds: IMEC (WP5 - Task 5.4)

Task Leader: IMEC

Contributing partners: KIT

Partner Contributions:

- IMEC: Design of filters
- KIT Design of filters

Task 5.4 Signal generation module design [M4-M12]

The aim of this task is to produce the functional specification, to implement (VHDL design, FE netlist) and to verify the Dual Die Communication Module (DDCM), the digital electronic module to generate electrical data signal to test plasmonic chip to chip communication platform in Systems in Package (SiPs); in a first phase the DDCM will be implemented so to be integrated with a *classical* electrical PHY, while in a second phase it will be generalized and enhanced in order to allow the implementation of a full *in-package network*, going beyond the limited scenario of chip to chip communication. In this context it's foreseen also the specification, implementation and characterization of encoding/decoding modules aiming at reducing the switching activity over the physical channel, so to reduce dynamic power consumption during transmission between the optical devices and detecting and correcting transmission errors, according to the forecast stating that with CMOS technologies such as 22nm and below transmission cannot be considered error free anymore (BER > 10^{-15}):

Fed by: WP2-task 2.1, WP3-task 3,1, 3.2

Feeds: WP6-task 6.3

Task Leader: ST

Contributing partners: ST

Partner Contributions: IMEC, KIT

- ST will produce architecture specification of an off-chip communication system enabling SiP.
- ST will produce full functional VHDL code and FE netlist able to operate with both traditional electrical PHY and plasmonics-based PHY.
- ST will produce a set of HW components (both VHDL and FE netlist) implementing

channel encoding/decoding techniques for ensuring low power chip to chip communication.

- ST will produce a set of HW components (both VHDL and FE netlist) implementing error detection and correction techniques for ensuring safe chip to chip communication.
- IMEC will provide specifications regarding the optical interface
- KIT will provide specifications regarding the electrical interface

Task 5.5 Signal Generation Module implementation via FPGA[M13-M24]

The aim of this task is to produce a hardware version of the DDCM specified and designed in task 5.4 exploiting FPGA technology; the specification of a simplified (low performance) version of serializer/deserializer is required in order to map these blocks, usually analog, into a digital FPGA. This will allow a more realistic validation and characterization of the plasmonic interconnect modules with respect cosimulation with CMOS FE netlist.

Fed by: WP5 - Task 5.4

Feeds: WP6 - Task 6.3

Task Leader: ST

Contributing partners: ST, IMEC, KIT

Partner Contributions:

- ST will implement the Signal Generation Module as hardware exploiting FPGA technology
- IMEC will provide the design for the optical interface
- KIT will provide design for the electrical interface

WP6 – Integration Characterization, and testing

Objectives

The objective of this WP is:

- The characterization and testing of the particular active and passive plasmonic devices.
- Its integration with the plasmonic interconnect modules, representing the physical layer (PHY) of such a communication structure and
- The System in Package characterization and testing

Description of work

The work-package will be led by ST and split in the following tasks:

Task 6.1 Characterisation of active and passive plasmonic devices [M7-M33]

In this task we will test and characterize all the active plasmonic devices such as plasmonic laser, modulators, amplifiers and photodetectors. The plasmonic waveguide-plasmonic couplers of Task 5.1 and the noise filters of Task 5.3 will be characterised using standard waveguide transmission measurement setups available at KIT resp. IMEC. For characterising the beam shapers (Task 5.2), IMEC will further expand an existing setup being developed for characterizing optical phased array antennas.

Fed by: IMEC, UVEG, KIT (WP3, WP4, WP5)

Feeds: KIT (WP3, WP4, WP5 and Task 6.2)

Task leader: AIT

Contributing partners: TUE, IMEC, KIT, UVEG

Partner Contributions:

- AIT: will define the testing procedures and the required characterization data that need to be collected and provide feedback to studies in WP2
- TUE: will perform plasmonic laser characterisation
- KIT: will perform plasmonic modulators characterisation
- IMEC: will perform plasmonic photodetector characterisation
- UVEG: will perform plasmonic amplifiers characterisation

Task 6.2 Assembly and packaging of plasmonic devices into System in Package [M30-M36]

Following the characterization, the transmitter and receivers will be assembled and packaged into a single device. Two SiP will be tested. The direct free space link and the fiber coupled link.

Fed by: IMEC, UVEG, KIT (WP6 – Task 6.1)

Feeds: KIT (WP6 – Task6.3)

Task leader: KIT

Contributing partners: KIT, ST

Partner Contributions:

- KIT: assembly, fiber-pigtailing, free-space packaging
- ST will support this activity

Task 6.3 Plasmonic chip to chip interconnect prototype testing and evaluation [M32-M36]

The aim of this task is to implement and characterize both individual plasmonic devices developed according to what described in the other WPs, and a prototype of the plasmonic interconnect, built by integrating the devices previously mentioned.

Fed by: WP3, WP4, WP5

Feeds: WP - Task 6.4, WP7

Task leader: AIT

Contributing partners: KIT; AIT, ST

Partner Contributions:

- KIT will participate in packaging.
- AIT will participate in testing and characterization of plasmonic interconnect prototype.
- ST will carry out an analysis on the developed chip to chip interconnect.

Task 6.4 System-in-Package integration and characterization [M22-M36]

The objective of this task is to implement a simple but complete SiP, exploiting some building-blocks already available in ST with the new modules and models being the outcome of task 6.3, 5.4 and 5.5, in order to carry out feasibility study and performance evaluation; in particular a characterization in terms of area, timing, power and performance will be carried out, as well as a comparison (benchmarking) with an equivalent system implemented with a traditional electrical PHY, in order to clearly state the advantages brought by this novel technology.

Fed by: WP2, task 6.3

Feeds: WP5 - Task 5.4, Task 5,5, WP7

Task leader: AIT

Contributing partners: ST, AIT

Partner Contributions:

- ST will assembly all the building-blocks coming from previous tasks and generate a system top level that will be simulated and characterized, and then passed to WP2 for benchmarking.
- ST will assembly all the building-blocks coming from previous tasks and generate a system top level that will be simulated and characterized, and then passed to WP2 for benchmarking.
- AIT will participate in testing and characterization of plasmonic interconnect prototype.

WP7 – Exploitation and Dissemination

Objectives

This Work package deals with the exploitation and dissemination of the developed optical interconnection platform, as well as the contribution to standardization bodies and promotion of the project to students and researchers within the scientific community and the general public.

The objectives of this work package are listed below:

- Identification of potential groups of users of the developed plasmonic devices technologies and establishing the chip-to-chip interconnection interface.
- Generation of intellectual property (patents portfolio) to set the basis for potential

commercialization of products relevant to the project results.

- Promotion of the project outputs through the participation in optical conferences and symposiums. Preparation and distribution of technical brochures.
- Dissemination of project results through publications in scientific journals and magazines, presentations in international conferences and workshops as well as through lecture presentations in academia and industry. Industrial partners should be present at related industrial meetings to promote the technology transfer.
- Monitor roadmaps and standards.
- Coordinate Activities towards possible contributions to standardization bodies (e.g. IEEE, ITU/FSAN).
- Interaction with other EU and National projects.
- Provide input to industrial partners based on scenarios of the proposed solutions.
- Maintenance of the project web site which will be used for information and result dissemination purposes. Public project reports will be made available there. The web site will have a specific section in the webpage dedicated to Innovation and Technology transfer and will provide means to allow for discussion and the possibility for others to submit information.
- Compile a regularly updated database of contacts that can be interested in the specific area including also a network of journalists/editors that can be interested in promoting the results of the project in their respecting newspapers/magazines.

Description of work

The work-package will be led by AIT and split in the following tasks:

Task 7.1 Dissemination of results [M 01-M 36]]

A detailed dissemination plan will be provided shortly after the project starts, which details the target groups and the dissemination method. Preliminary plans for dissemination are listed below:

a) Spreading the new technology platform and making it available
b) Dissemination through paper submission to high quality and high impact scientific journals and conferences.
c) Feeding supporting material to the industrial partners aiming to standardization bodies. [ST]
d) Supporting cluster and concerted activities in the EC framework program [AIT]
e) Through the web site [KIT].
f) Organising workshops and contribution to European magazines [AIT, after M24].
g) Demonstration activities [ST].
h) Issuing press releases [M02, M18, M36]

Fed by: WP2-WP7

Feeds: public

Task leader: AIT

Contributing partners: All

Partner Contributions:

- AIT: will lead the dissemination activities and define the actions for the dissemination of the project results.
- KIT: Dissemination of results by publication
- IMEC: Dissemination of results at conferences and journals.
- TUE: Dissemination of results at conferences and journals.
- UVEG: Dissemination of results at conferences and journals.
- ST will contribute in the dissemination and demonstration of results at conferences and exhibitions

Task 7.2 Exploitation of results [M12-M36]

The main objective of this task is to explore the research outcomes of the NAVOLCHI project and to promote market penetration of the end products. This task will be largely supported by industrial partner of the consortium who will play a key role in the product commercialization activities.

In particular this task aims:

a) To secure intellectual property of the research outcomes and, if appropriate, generate a patent portfolio.
b) To exploit the performance evaluation reports of the new technology with respect to the cost and power consumption benefits by creating manufacturability plans to pave the way for potential product commercialization.

Fed by: WP2 – WP7

Feeds: European Industry

Task leader: IMEC

Contributing partners: KIT, IMEC, TUE, UVEG, ST

Partner Contributions:

- KIT will contribute by patent filing
- IMEC will provide industrial expertise in the evolution to an R&D and manufacturing programme
- TUE will participate by securing IP
- AIT will evaluate the results of the studies from WP2 and will perform feasibility studies with respect to industrial product roadmaps. AIT will contact European industry to form an industrial board for commercial activities.
- UVEG will participate by securing IP
- ST will contribute to identify the best ways to protect the results by patenting and licensing, as well as to commercialize the optimized device parameters for optical interconnects.

Task 7.3 Promotion of Results [M24-M36]

This task has the objective to spread the knowledge gained during the project to the students and researchers of the scientific community as well as to inform them about the potential of these new technologies. This will be accomplished by the following activities:

a) Organization of a workshop on possibilities related to the new technology.
b) Lab visits and demonstration activities under the organization of a summer school.
c) Research problems can constitute the subject of student theses/projects.

d) Appropriate results from this project will be fed into the Jeppix Optical chip design course which is held at the TU/e and has attendees from around the world

The aim is to organize a summer school with lab visits after the end of the second year and a workshop during the third year.

Fed by: WP2-WP7

Feeds: -

Task leader: AIT

Contributing partners: KIT, AIT, ST

Partner Contributions:

- KIT and AIT will contribute to workshops
- AIT and KIT will contribute to the organization of the summer school.
- ST will contribute with their knowledge and long-term experience in chip-to-chip interconnects environments.
- TUE will organise Jeppix Optical chip design course.

B1.3.4. *Pert diagram of the components and their interdependencies*

The Pert diagram of the components and their interdependencies is shown in Figure 1.3.12, which show how the plasmonic chip-to-chip interconnect system, design and modelling, fabrication, characterization and evaluation are organized. Input from WP2 is passed on to the design and fabrication of plasmonic transmitter, receiver, optical and electrical interfaces in WP3, WP4 and WP5, respectively and then is passed on the WP6 where the entire devices are characterised and integrated. Finally, the test and evaluation of the integrated chip-to-chip interconnects is performed in WP6. Results are communicated to WP7. Management communicates with all WPs.

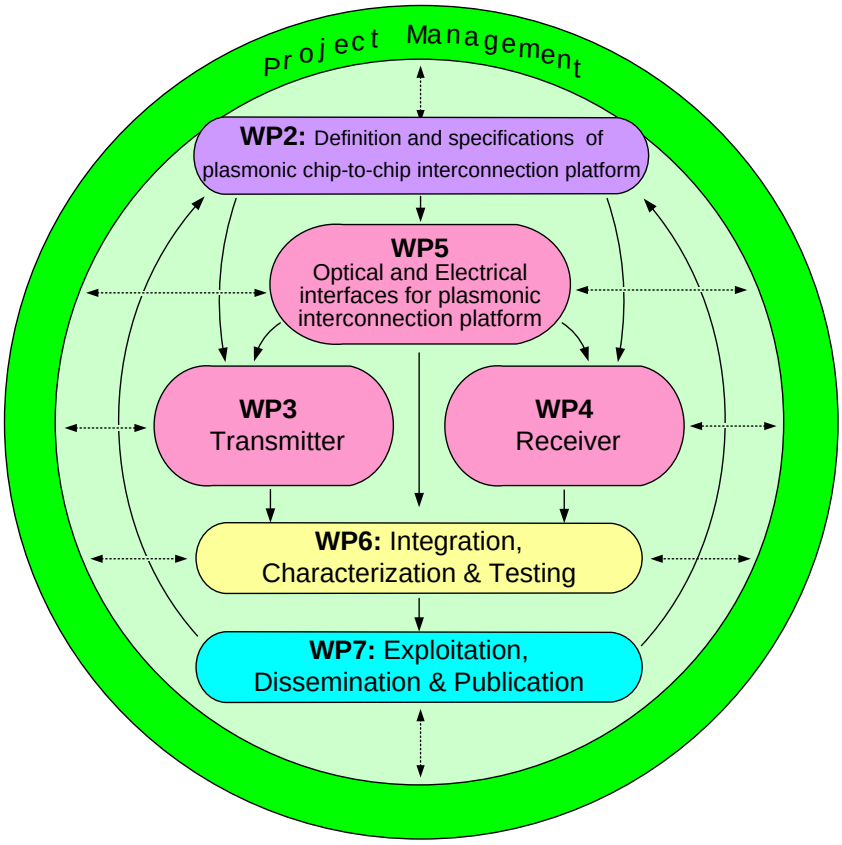


Figure 1.3.12 Pert Diagram of the Project

B2. IMPLEMENTATION

B2.1. Management structure and procedures

This section provides details about the organisational structure and decision-making mechanisms of the project.

B2.1.1. *Management capability of the co-ordinator*

A simple Project Management structure adapted to the project size has been agreed among the partners and is shown in Figure 2.1.1. Additionally, Figure 2.1.1 shows the information flows between the European Commission and the project.

The project consortium is led by the **General Assembly (GA)** and the **Project Management Committee (PMC).** These two governance bodies are in charge of the administrative and technical aspects of the project, respectively. An **IPR Audit Committee** may be added ad-hoc for resolving IPR related issues. The technical work is organized around **work packages (WPs).**

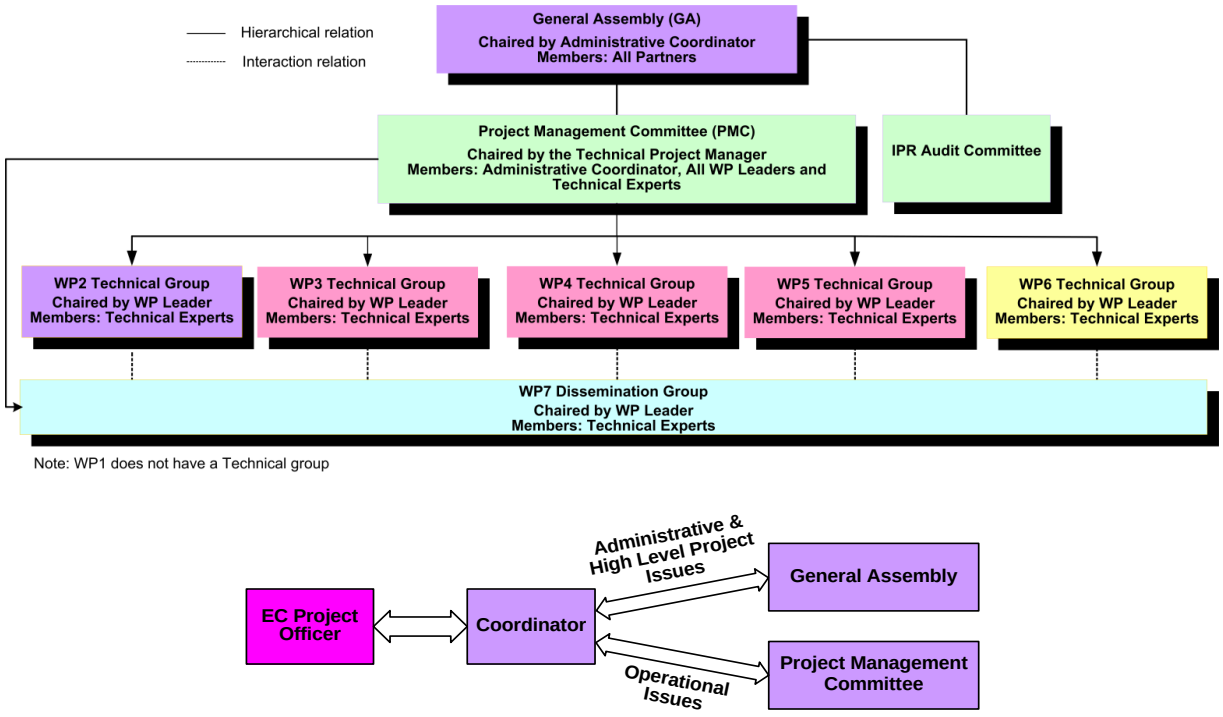


Figure 2.1.1 Information flow between the European Commission and the project

Four documents produced at the project start will establish the rules of project management:

The mandatory Consortium Agreement (CA) shall, among others, describe in detail the composition, decision making procedures and responsibilities of the Project Coordinator, General Assembly, and Project Management Committee.

The Reference Online Manual will set the day to day rules of the project: documents and deliverables handling, project planning and manpower, meeting organization, internal reporting and information management, external information management, list of personal with corresponding responsibilities. The document will be updated throughout the project life.

The Project Quality Online Assurance Manual will define the quality assurance and quality control rules and guidelines to follow, including documentations and information to provide and the different internal milestones in the R&D process, and change control procedures.

The Knowledge Management Guide which details, beyond the terms of the EC grant agreement, the internal project rules and guidelines concerning the management of foreground and IPR. The role of the different organizational bodies will subsequently be described.

The General Assembly (GA)

The role of the General Assembly is to ensure a follow-up of the project and to take the major decisions relative to the project. The role and responsibilities of the General Assembly are detailed in the Consortium Agreement (based on DESCA model[62]). They are the following:

Contract and consortium agreement amendment;

Termination of the contract and actions against defaulting partners;

Selecting new contractors to enter contract & consortium agreement;

Deciding major changes in the project;

Budget follow-up and transfers;

Deciding on technical roadmaps for the project;

Approval of certain decisions of the Project Management Committee.

The General Assembly shall comprise one representative of each Partner. Each Partner shall nominate a senior representative, with budget responsibility, enabling to make consistent decisions and to represent contractor's interests. The General Assembly shall be chaired by the Administrative Coordinator.

The GA shall be convened by default every year. The ordinary GA meetings shall be convened together with a project meeting. An extraordinary General Assembly meeting can be called at any time by the Administrative Coordinator or any partner under the terms and rules of the Consortium Agreement. In case of urgent conflict resolution, GA can take decisions by conference call, e-mails procedure as described in the CA. Decisions will be taken by consensus whenever possible; only in case of conflict and decision will be taken by voting. In voting each Partner shall have one vote. In case of a tie result the Administrative Coordinator gets an additional vote. Partners, leaving the project, will loose their representative and their vote in the GA. If a new partner enters the NAVOLCHI consortium, the GA will decide about his level of representation in the GA.

The NAVOLCHI Project Management Committee (PMC)

[62] http://www.digitaleurope.org/index.php?id=32&id_article=163

The Project Management Committee has the responsibility for the overall project progress and results in full conformance with the decisions of the GA. The main responsibilities of the PMC are to monitor the overall project progress (objectives, schedule, milestones, etc), to discuss and agree on actions in case of deviations from project plan, and to approve project deliverables and any changes of legal project documents if necessary. The responsibilities of the Project Management Committee will address the following issues:

Coordination, monitoring and control of the progress of the work in the project,

Launch or stop of Work-packages,

Technical Management of the project:

Analyses and solutions on technical issues,

Technological roadmaps,

Approval of the deliverables

Launch selection of sub-contractors

Preparation of dissemination and communication with the support of WP7,

Management of foreground and IPR,

Publications and press releases.

The Project Management Committee shall consist of:

The NAVOLCHI Technical Project Manager (will be elected upon the project start date).

The Administrative Coordinator (Prof. Juerg Leuthold of KIT)

The WP Leaders

WP7 leader when necessary for dissemination purposes

Additional Technical Experts from the WPs that will be elected upon a need base

The PMC can be renewed by the GA under the terms of the Consortium Agreement. Physical meetings of the PMC are organized every 4 months. In between teleconference are organized every 2 months or on request (in accordance with the CA rules).

Decisions will be taken by consensus whenever possible. No voting will occur within the PMC In case of conflict or for decisions beyond PMC responsibilities, the PMC will refer to the GA.

Work Package Technical Group

The WP technical Group is composed of all the members of the WP and is chaired by the WP leader. The WP Technical Group takes the technical guidelines from the Project Management Committee, makes further technical choice to implement these directives and produce the deliverables.

WP1 does not have its own technical group as WP1 matters are treated by the PMC.

WP7 has also a particular role: it is to handle all issues related to the communication of the project with the research community, the industrial world, the standardization bodies and the academic community.

The WP technical group is composed of the WP leaders and all partners' members working in the WP

WP Technical group meetings occur at the same place and location as PMC meetings. They are convened before the Project Management Meeting, to enable reporting and resolution of issues there. In addition, Work package Technical Group (WP) meetings can be called and organized by the WP leaders when needed for the good progress of the technical work. All decisions are consensus driven; no voting is allowed. Decisions that cannot be solved at the WP level will be escalated to the PMC, then to the GA where a vote would occur.

IPR Audit Committee (IAC)

The IPR (Intellectual Property Rights) Audit Committee is a small group, which shall meet upon request and need by the General Assembly or its members. The IPR Audit Committee assesses all IPR relevant information that was brought in the project or was developed within the project. Based on the ownership of IPR, access rights and use of results shall be determined and regulated. The IPR Audit Committee gives recommendations to the General Assembly on the handling of the assessed IPR issues. The IPR Audit Committee shall consist of a maximum of five experts with IPR background recruited from the consortium partners. The General Assembly decides about the composition of the IAC.

B2.1.2. *Management structure and decision-making structure*

The Administrative Coordinator co-ordinates the activities of all partners in the project according to work plan, and provides the Commission with technical, managerial and financial information. He will act as the unique focal point for contacts and co-ordination with the European Commission, with other relevant IST projects, and external relationship with relevant bodies and other related activities. More particularly he is in charge of representing the GA reporting to the commission and interfacing the EC Project Officer, and reporting to GA about all administrative issues emerged by the EC Project Officer. The Project Administrative Coordinator chairs the General Assembly. His major tasks are:

- Supervision of the overall project progress
- Consortium Agreement coordination
- Collection of the audit certificates and supervision of distribution of EC's payments to partners
- Preparation with the support of the Project Management Committee of the reports, cost statements and project documents required by the EC
- Organisation of EC review meetings
- Supervision of IPR and knowledge management (with relevant advice of IPR Audit Committee)
- Representative of the consortium to events
- Coordination of the dissemination and communication activities

The project Administrative Coordinator is supported in the above tasks by the Technical Project Manager. The Administrative Coordinator will be Prof. Juerg Leuthold (KIT) for the NAVOLCHI Project.

Technical Project Manager

The Technical Project Manager will be elected upon the project start and he will have the following responsibilities:

Chair of the Project Management Committee

Liaisons between the Project Management Committee and the General Assembly

Technical relationship and coordination with other relevant R&D projects

Supervision of the overall technical progress of the project

Consolidation of the technical reports

Preparation of minutes of the General Assembly, and follow-up of its decisions

Follow-up and coordination of all technical work-packages

Transmission of any documents and information connected with the project between the partners

The Technical Project Manager is assisted in all the non-technical tasks by the Administrative Coordinator.

WP Leaders

The WP leader is designated by the Project Management Committee. Preliminary WP leaders have been already assigned:

WP1 is KIT led by Prof. Juerg Leuthold

WP2 is AIT led by Dr. Dimitrios Klonidis

WP3 is TUE led by Prof. Martin Hill

WP4 is UVEG led by Prof. Juan P. Martinez Pastor

WP5 is IMEC led by Prof. Dries Van Thourhout

WP6 is ST-i led by Dr Alberto Scandurra

WP7 is AIT led by Prof. Ioannis Tomkos

The responsibilities of the WP leader are:

To manage and follow-up the progress and technical activity of the work package

To follow-up the timely achievement of milestones and production of deliverables

To report on the activity to the Project Management Committee

In case of conflict within the WP, the WP leader will report the issues to the PMC and propose solutions.

B2.1.3. *Communication strategy*

Meetings and Travel management

Meetings are organised at a frequency defined above. In order to minimise travel costs, the partners agree to meet 2 to 3 days every 4 months in Joint Consortium Meetings. During these days, all meetings of the various bodies will take place. Ad-hoc meetings for integration, test, or solving special issues can be organised in addition to the regular meetings. At the project start, the PMC (Project Management Committee) issues the calendar (time and place) of the various meetings for one year, and from then, one year in advance.

Planning

Drafting coherent plans for the Project work is an essential prerequisite to enable the work to progress. The current document only presents a high-level overview of the Project, setting out the ground rules on which the Project will proceed in terms of objectives, technical approach and time scales. At the project start a consolidated planning will be produced, and will be maintained by the Administrative Coordinator.

The work plan described in the planning is the basis on which both WPs and Partner progresses are judged and reported. The work plan can be revisited only with the approval of the PMC.

Deliverables

Complete deliverables handling and approval procedures will be defined in the Project Management Manual. Deliverables consist in reports, white papers, documents, laboratory models, evaluations, field trials, etc. They are first approved by the WP leader, and then by the Technical Project Manager after review by appointed reviewers. Reviewers are named by the Project Management Committee, and are usually internal to the project. The reviewers submit their findings and recommendations in writing to the WP leaders and the Project Management Committee. The latter has the final authority on the deliverable and responsibility for its quality.

The NAVOLCHI Website

The Consortium will use for its communication an interactive web site both for internal and external communications. This site is secured and enables the Consortium to manage the diffusion of the information and exchanges between partners. The main communication components of this tool are: generation of highlights, presentation of the management data and their evolution (manpower, financial, deliverables, partner contact persons, Gantt charts, etc.), organisation of meetings, document library, forum of discussion, etc.

The site is on-line accessible by the Commission for the project official documents. The same site publicly disseminates results and progress of NAVOLCHI. The different user groups have different access levels to this site.

Conflict resolution

The clear decision making procedures described in 2.1.2 allows a simple conflict resolution process. When a conflict occurs in a WP technical group, consensus seeks to solve the problem. If the problem cannot be solved it is escalated to the Project Management committee: the WP leader prepares a description of the problem and its possible solutions. If consensus cannot be reached within the Project Management Committee, the Technical Project Manager escalates it to the GA, using the same process as described above. If the problem cannot be solved by consensus, vote will occur, requiring a simple majority. In practice the conflict resolution process can be very fast, as:

Extraordinary Project Management meetings and GA meetings can be organised using audio conference (with the terms and delay defined in the Consortium Agreement)

Email voting is allowed (again according to the rules defined in the Consortium Agreement).

B2.1.4. *Monitoring, reporting progress and documenting results*

Progress reports

The progress reports shall provide a tabular comparison between targeted, achieved performance and the state-of-the-art. Each partner writes a milestone, intermediate progress and periodic report to the WP leaders with copy to the coordinator. The milestone report is typically a two to three page document. The intermediate progress and periodic reports describe the technical progress and management project work done, listing their names and effective time spent on the project. It mentions difficulties, milestones and deliverables (or contributions to deliverables in case of joined deliverables) that have been reached, patents, publications, travel and visits. In addition, the periodic reports (M18, M36) have to include an Expenses Report to the Technical Project Manager summarising all costs that have been incurred, with quantitative inventory of spent manpower and expenses. The intermediate progress and periodic reports will be sent to the EC. The milestone reports will be collected and sent to the EC as an attachment to the intermediate progress and periodic reports.

Reports to the Commission

The Project Administrative Coordinator (with Technical Project Manager) will co-ordinate and consolidate intermediate progress (M09, M27), periodic (M18, M36) and final reports, which need to be submitted to the Commission. Every Partner will provide audit certificate when needed (according to FP7 rules) prepared and certified by an external auditor selected by the Partner, certifying that the costs incurred during the period meet the conditions required by the grant agreement.

Quality approach

Quality shall not only be addressed for the Deliverables but also for the Project process itself. The management process shall be submitted to periodical reviewing with respect to:

Adequacy of the project management plan and how the work performed complies with it, including IPR management and results dissemination,

How well the project processes are synchronized and inter-linked,

Identification and evaluation of activities and results that would adversely affect the achievement of the project objectives,

Process improvement in the project by identifying deviations and changes.

A Quality Assurance Plan will be developed within WP1 (Management) in month 3. The plan will be applied to all internal and external services and deliverables. Quality assurance is the joint responsibility of all partners and will be applied at all levels of the project's activities.

Management will continuously monitor and control (i.e. taking corrective actions) expenses, resources and schedules versus plans (i.e. technical and financial annexes to the EC Grant Agreement). A list of precise success criteria for the project will be set up and maintained during the project life.

Root causes for deviations, be it shortages or excesses, in costs, resources and schedules shall be identified, recorded and used as input for continual improvement.

Possible impacts of schedule changes on the budget and resources of the project and on the quality of the product should be determined.

Deliverables prepared by any person of the project will be first reviewed and then submitted to approval following a defined process that will be described in the project management manual.

Management of Knowledge and Intellectual Property

From an organizational point of view, knowledge management and management of innovation related activities, issues with IPRs, including exploitation of results and business creation will be handled by the Project Management Committee. More details can be found in Chapter 3.2.3 on page 101.

A Knowledge Management Guide including procedures is produced in month 6 by the project management for the NAVOLCHI partners. Knowledge management issues will be on each Project Management Committee agenda. For specific cases assistance will be sought from high-level experts recruited from the participants of the consortium (within the IPR Audit Committee).

Risk management and mitigation

Risk may arise from technical issues, by difficulties in collaborations with partners or by the mere fact the some partners might drop out due to economic issues. We have outlined those risk and the respective contingency plans in section 1.3.6.

Documentation

Document management rules and guidelines will be contained in the Project Management Manual produced by WP1 at the project start. The usual tools (Fax, E-mail, FTP Server, and Web Server) will be used for the exchange of documents/information. They will be complemented when needed by audiovisual conference systems. Internal (or external) meeting documentation including discussion and information notes will be distributed to each participant and published on the Web server of the project.

Document produced by the project will be properly managed, with reference to the Project Management Manual:

Usual electronic formats will be explicitly agreed upon a structured identification and version reference will be given to each of them indicating:

Type (ex. Deliverable, Internal document, Published document, etc.)
Status (e.g.; planned, draft, distributed, approved, living, final, obsolete, etc)
Confidentiality level (e.g. public, Consortium only, strictly confidential, etc)

B2.2. Beneficiaries

A balanced and interdisciplinary consortium consisting of five research centres and a large company has been formed. All of the respective partners contribute to the project within their area of expertise.

B2.2.1. *Karlsruhe Institute of Technology (KIT)*

Partner description and experience

The Karlsruhe Institute of Technology (KIT) is the oldest technical university in Germany and belongs to one of ten elite universities in Germany. The KIT has an approximate 20000 students and one of the highest external research funding in Germany. The Institute of Photonics and Quantum Electronics (IPQ, www.ipq.kit.edu) has approximately 40 members. The IPQ works in the field of photonic material sciences and optical communications with a particular emphasis on nonlinear optics, silicon photonics, plasmonics and novel modulation formats. The IPQ has a broad experience with European and National projects. The IPQ has been or currently is coordinating the European research projects TRIUMPH (Tbit/s router with channel rates from 10 to 130 Gbit/s) and SOFI (on silicon-organic hybrid modulators). The IPQ is further a partner of the European network of excellence EUROFOS and the EU project ACCORDANCE. Within Germany, the IPQ substantially contributes to national BMBF (German Federal Ministry for Education and Research) projects, such as MISTRAL (a silicon on insulator project) or to CONDOR, where OFDM access networks are developed. The IPQ is further involved in many other programs such as the "DFG Functional Nanostructure" research initiatives, research activities with the Deutsche Telekom and Agilent. The IPQ is an "affiliate partner" of the European ePIXnet network.

Role in NAVOLCHI Project

KIT will be the Project Coordinator of NAVOLCHI project. In WP3 KIT will contribute the plasmonic modulator design for the development of plasmonic transmitter. The KIT will fabricate the plasmonic modulator via performing postprocceising steps on a SOI chip. The modulators will be characterized at the labs of IPQ. Within the framework of WP5, the KIT will develop passive components, particularly plasmonic couplers and filters as well as suitable plasmonic waveguides for plasmonic amplifiers within the WP4. The KIT will be also involved in the dissemination activities within WP7.

Key personnel contributing to the project

Prof. Dr. Juerg Leuthold is the head of the Institute of Photonic and Quantum Electronics (IPQ) and of the Institute of Microstructure Technology (IMT) at the KIT. He has graduated from the Swiss Federal Institute of Technology (ETH) in 1998, spent a postdoc time at the University of Tokyo (1999) and was with Bell Labs, Lucent Technologies in New Jersey from 1999 to 2004 before he became a full Professor in Karlsruhe. Juerg Leuthold is a fellow of the Optical Society of America (OSA), and the youngest member ever elected to the Heidelberg Academy of Science. He has been the general chair of the OSA Advanced Photonics Congress 2010 and has been or is serving the community as a TPC member for OFC, ECOC, CLEO and many other meetings.

Prof. Christian Koos is professor at Karlsruhe Institute of Technology, Institute of Photonics and Quantum Electronics (IPQ) since 2010. His present research activities are in the fields of high-density integrated photonic systems, silicon-organic hybrid integration, and ultrafast optical signal processing. He received the PhD from the University of Karlsruhe in 2007. From 2007 to 2008, he carried out post-doctoral research at the IPQ of the KIT. From 2008 to 2010, he was leading the technology radars "Nanotools and Nanometrology" and "Metrology" within the Corporate Research and Technology department of Carl Zeiss AG, Germany.

B2.2.2. *Interuniversity Microelectronics Centre (IMEC)*

Partner description and experience

IMEC was founded in 1984 by the Flemish Government. It stands out as the largest independent European research centre in the field of microelectronics, nanotechnology, enabling design methods and technologies for Information and Communication Technology (ICT) systems. Today, IMEC has a staff of more than 1750 people, including 550 guest researchers and industrial residents. It is more than 120 million EURO revenue is derived from agreements and contracts with the Flemish government, the EC, EUREKA, the European Space Agency, equipment and material suppliers and semiconductor companies world-wide. IMEC performs scientific research that runs 3 to 10 years ahead of industrial needs. Its balance between basic and application oriented research and its IPR policy form an attractive base for world-wide industrial collaborations.

The silicon photonics research group (about 60 people) of IMEC is headed by Prof. R. Baets and has been active in optoelectronics and photonics devices for many years. The main applications under study are silicon nanophotonics, heterogeneous integration, optical interconnect within advanced electronic systems, WDM optical communication, silicon photonics biosensors and biomedical applications. More in particular, the silicon nanophotonics work focuses on the design and fabrication of SOI-based photonic crystal structures, photonic wires and fiber-coupling structures using standard lithographic techniques compatible with CMOS-processing. The group is also strongly involved in the development of heterogeneous technologies, whereby the silicon photonics platform is combined with other materials such as III-V semiconductors for efficient sources, nanocrystals and polymers. The group has been the prime contractor or contributor for numerous EU-projects, including the FP7 projects WADIMOS, BOOM, SMARTFIBER, SOFI and INTOPSENS. Through ePIXfab (funded through the EU-project Photonfab), IMEC is providing its silicon photonics technology to over 50 research groups all over the world using a cost-effective multi-project approach.

Role in NAVOLCHI project

IMEC will provide the basic silicon photonics circuits needed to form the interconnect backbone connecting the different plasmonic devices with low loss. In addition, IMEC will develop an electrically injected integrated optical amplifier based on colloidal nanocrystals, embedded in a hybrid silicon-plasmonic device.

Key personnel contributing to the project

Prof. Dr. Ir. Dries Van Thourhout spent two years at Bell Laboratories, Crawford Hill, working on InP-based multi-wavelength devices. He is currently responsible for the processing facilities within the photonics group at IMEC-INTEC. His research interest includes monolithically and hybrid integrated optoelectronic devices, multi-wavelength lasers and heterogeneous integration. He has been the coordinator of the IST-PICMOS project and is currently coordinator of the IST-WADIMOS project. He is holder of an ERC starting grant.

Prof. Dr. Ir. Wim Bogaerts is Professor in the Photonics Research Group of IMEC-Ghent University. He obtained his PhD in 2004 on silicon nanophotonic waveguide structures and since then coordinates the joint silicon photonics developments between Ghent University and IMEC. His

research involves novel silicon photonics, from new design methodologies over new process developments, components to specific applications.

B2.2.3. *Ghent University (UGent)*

With over 30.000 students, Ghent University is now Belgium's largest university. Over the years eminent scientists such as Joseph Plateau (physicist, considered as a pioneer in the development of motion pictures), Leo Baekeland (inventor of Bakelite) and Corneel Heymans (Nobel Prize winner in Medicine) studied and worked at Ghent University. With a view to cooperation in research and scientific service, numerous research groups, centres and institutes have been founded over the years. Several of them are renowned worldwide, in various scientific disciplines such as biotechnology, aquaculture, microelectronics, photonics, history. Today, after decades of uninterrupted growth, Ghent University is one of the leading institutions of higher education and research in the Low Countries. Ghent University is an open, committed and pluralistic university with a broad international perspective.

The physics and chemistry of nanostructures group at Ghent University was established in 2002 by prof. Z. Hens. In less than 10 years, it has become a multidisciplinary research group with 2 professors (by 01/10/2011), and 10-15 PhD students and postdoctoral researchers. The main focus of its research is the synthesis and processing of colloidal nanoparticles – especially colloidal quantum dots – their structural and opto-electronic charcacterization and their applications as emitters or absorbers of light. The group has a wider range of national and international collaborations, both with academic research groups and industrial partners. It is involved in several national research networks, and in the EU FP7 integrated training network Herodot.

Role in the NAVOLCHI project

UGent will contribute in the synthesis of PbS(e), PbS(e)/CdS(e) core-shell dot-like and rod-like quantum dots, in the preparation and processing of quantum dot or quantum dot doped layers and in their optical and electrical characterization.

Key personnel contributing to the project

Prof. Dr. Ir. Zeger Hens leads the Physics and Chemistry of Nanostructures Group at Ghent University. He recieved his PhD in applied physics from Ghent University in 2000 and subsequently spent 2 years as a postdoctoral re-searcher at Utrecht University. His research focuses on the synthesis, electro-optical characterization and application of advanced nanomaterials such as colloidal quantum dots.

B2.2.4. *Technische Universitet Eindhoven (TUE)*

Partner description and experience

TU/e Technische Universiteit Eindhoven University of Technology

The Eindhoven University of Technology hosts the COBRA Research Institute; the Dutch national centre on III-V-semiconductors and opto-electronics and one of the six top research schools in the Netherlands. It is one of the world's best equipped academic research

centers in the field of Photonics, with an 800 m^2 cleanroom, a variety of epitaxial growth and characterization facilities and the full suite of lithography and processing equipment for III-V semiconductor based devices. Further COBRA has an extensive infrastructure for ultra-high speed characterization of devices and systems. It provides access to its integration technology to other European Universities in the framework of the European Platform for Photonic Integration of Components and Circuits JePPIX. In the last decade it has participated in more than 15 European research projects.

Role in NAVOLCHI project

At the TUE the Opto-Electronic Devices group (OED) plays a leading role in the development of advanced Photonic ICs. In 2007 it reported the first electrically injected metallic nanocavity laser. More recently in 2009 it also reported the first Plasmon mode lasers with nano scale confinement of light. In particular the OED group concentrates on electrically pumped metallic/plasmonic nano-laser devices, which at this moment is unique in the world. In the project the OED group will use its plasmonic nano laser technology and simulation expertise to develop nano-scale metallic/plasmonic laser sources which are bonded onto SOI wafers.

Key personnel contributing to the project

Martin Hill is professor of nano-photonic integration at the Opto-Electronic Devices group of TU Eindhoven. He has expertise in InP based Photonic Integrated Circuits. Furthermore he has been investigating the use of lasers for optical signal processing and switching of telecommunications data over the last decade. More recently he has focused on the further miniaturization of semiconductor lasers via metallic and plasmonic nano-cavities. In 2007 he was the first to demonstrate that lasing was possible in metallic nano-cavities. He has authored or co-authored more than 100 journal and conference contributions.

B2.2.5. *Research and Education Laboratory in Information Technology (AIT)*

Partner description and experience

Research and Education Laboratory in Information Technologies (AIT) is a centre of excellence in ICT research and graduate education. AIT participates in NAVOLCHI project with its 'High-Speed Networks and Optical Communications' (NOC) research group. The group maintains a broad range of research interests, scientific and technical expertise related with high speed networking and a state-of-the-art laboratory to support innovative research activities on optical communications. The work carried out within the AIT's NOC group is focused on optical network infrastructures for existing and future broadband networks and services/applications support in access, metro and wide area networks. Specific areas of interest include novel architectures for circuit-, burst- and packet- switching, optical system and subsystem design, high bit rate transmission systems, advanced modulation formats, all-optical signal processing subsystems, switching techniques and techno-economic studies. The group's research activities are supported by a state of the art high tech laboratory with 10Gbit/s WDM system (to be upgraded to 40 Gbit/s) and recirculating loop capabilities. Moreover NOC lab includes many components like amplifiers, filters, MEMs etc. Additionally the NOC lab is equipped with commercially available S/W tools like: VPI Transmission, Transport, Access Maker, OPNET, and Matlab. The NOC

group is/has been involved in many EU projects (CHRON, ACCORDANCE, SOFI, DICONET, SARDANA, NoE BONE, APACHE, NoE EUROFOS, BReATH, TRIUMPH, NoE e-Photon/ONE2, COST 291 TDON). AIT will participate with a number of senior researchers with many years of industrial experience and a solid research background recognized through a number of more than 250 publications in international journals and conference proceedings and coauthored numerous technical reports in areas related with their field of expertise.

Role in NAVOLCHI project

AIT researchers will contribute in NAVOLCHI project with their expertise in system/subsystem design, performance evaluation studies. More specifically AIT will lead WP2 which will define the reference system design and will explore new emerging and potential applications based on the characteristic properties of the new disruptive plasmonic devices. In addition, AIT will evaluate the performance of the new hybrid technology components with respect to the delivery of new functionalities in high data rate transmission systems. The abovementioned study will be carried out based on the extraction of the device specifications though physical layer simulations. AIT, will also investigate the performance of the hybrid technology in the existing and the new applications in terms of cost efficiency and power consumption reduction capabilities. Finally, it will contribute to the final system testing and demonstration activities.

Key personnel contributing to the project

Prof. Dr. Ioannis Tomkos is with the Athens Information Technology Center (AIT) since Sep 2002 and an Adjunct Faculty at the Information Networking Institute of Carnegie-Mellon University, USA (2002-2010). In the past, he was senior scientist (1999 - 2002) at Corning Inc. USA and research fellow (1995 - 1999) at University of Athens, Greece. At AIT, he served as Associate Dean (2004-2009) and he founded and serves as the Head of the "High Speed Networks and Optical Communication (NOC)" Research Group that was/is involved in many industry and EU funded research projects (including 7 running FP7 EU projects) within which Dr. Tomkos is representing AIT as Principal Investigator and has a consortium-wide leading role (project leader/technical manager/workgroup leader). Dr. Tomkos has received (2006) the prestigious title of "Distinguished Lecturer" of IEEE Communications Society. Together with his colleagues and students he has authored over 360 scientific articles and presentations (over 190 IEEE sponsored items), including about 100 Journals/Magazines/Book chapters.

Dr. Dimitrios Klonidis is a senior researcher at AIT and responsible for the NOC group laboratory. His main research interests are in the area of ultra-fast photonic networks, including transmission. Modulation, switching, high speed optical processing and fast node control. The considered networking applications include high capacity SONET/SDH, Optical Packet/Burst Switched and Grid Computing.

B2.2.6. *University of Valencia (UVEG)*

Partner description and experience

The University of Valencia (**UVEG**) is known since 1499. Now it is one of the oldest, largest and most important universities in Spain and includes 92 departments and 16 research institutes. The research budget coming from regional, national and European

funding was 55 M€ in 2005. **UVEG** is the fourth university in Spain within the ranking of research.

The research Institute of Materials Science of the University of Valencia (ICMUV) was organized in 1995 from the union of several research groups of the Chemistry and Physics Faculties. Now, the institute has a research budget above 1 M€ per year and includes 28 permanent researchers and 24 PhD and post-doc researchers.

The Unit of Materials and Optoelectronic Devices (UMDO) within the ICMUV is leaded by Prof. Dr. Juan P. Martínez-Pastor, has now 2 permanent staff, 4 senior researchers and 8 PhD students and has an approximate budget above 250.000 € per year. Since 1999 the UMDO group (www.uv.es/umdo) conducts investigations of optical properties in quantum wires and dots, including optical micro-spectroscopy of single quantum dots and nanowires (since 2003). Since 2007 three new laboratories have been opened within the group to work in: 1) Growth of semiconductor nanostructures and metal nanoparticles by laser ablation, 2) Simulation-modeling, fabrication and characterization of photonic/plasmonic structures, 3) Organic synthesis of semiconductor and metal nanoparticles, nanocomposites and complex nanoparticles. In total, around 40 full-size articles have been published by the group members and 4 patents registered during the last 3 years.

European experience: (1) SANDIE (FP6, 2004-2008), Network of Self-Assembled semiconductor Nanostructures for new Devices In photonics and Electronics, UMDO was active in "Single Photon" and "Novel Nanostructures" workpackages; (2) POSITIVE (FP7, 1/9/2010-31/8/2013), Strep project entitled "A highly integrated and sensitive PORous SIlicon based lab on a chip for multiple quantitaTIVE monitoring of Food allergies at point of care"; (3) NANOPV (FP7, 1/2/2011-31/1/2014), Strep project entitled "Nanomaterials and nanotechnology for advanced PhotoVoltaics, to develop breakthrough solar cell processing flows for cost-effective manufacturing of solar cells partially or fully based on nanomaterials".

Role in NAVOLCHI project

UVEG team is the leader of WP4 and will be involved in some the most important tasks within this WP. In particular, the team will be strongly involved in the preparation of patternable polymer based materials doped with quantum dots in order to fabricate plasmonic amplifiers and photodetectors. Modelling, structural, morphological, electrical, optical and electro-optical characterization of materials and devices will be also developed by the team.

Key personnel contributing to the project

Prof. Dr. Martínez-Pastor obtained his degree and PhD in Physics by the University of Valencia in 1985 and 1990, respectively. Since 1994 he occupies a permanent position at the University of Valencia and became Full Professor in June 2008. His international experience includes 3 years of postdoctoral stays at the European Laboratory of Non Linear Spectroscopy (Florence, Italy) and at the École Normale Supérieure (Paris, France). He is specialized in Semiconductor Physics, particularly optical properties of quantum heterostructures and nanostructures based on III-V semiconductors. He is author/co-author of more than 120 research publications. Since 1998 he has supervised 6 PhD thesis, 11 master thesis, 3 end-of-degree works and is currently supervising other 7 PhD thesis projects, all of them in the research field of quantum nanostructures and photonic/plasmonic structures. Since 1996, he has leaded 7 national projects, 4 bilateral integrated actions (France, Tunisia, Morocco), participated in 1 European Network FP6 and recently participating in 2 Strep projects FP7.

Dr. Isaac Suárez is a posdoc researcher in the UMDO group. He has a degree in Telecommunication Engineering (2002) and PhD in Physics (2006), devoted to the implementation of integrated optic devices (lasers, modulators and biosensors) in $LiNbO_3$. In the period 01/04/07-31/03/09 he developed a posdoc stay at **LAAS-CNRS** related to the optimization of the **oxidation** of $Al_xGa_{1-x}As$ heterostructures, in order to improve the performances of VCSELs with integrated functions by means of finally tuned lateral confinement and to develop other integrated devices in **GaAs** like lenses, photonic crystals or integrated mirrors.

Prof. Dr. Alfredo Segura is Full Professor at ICMUV and head of the Semiconductor Physics Group. He is author/co-author of more than 160 research papers and has been advisor of 12 PhD theses.

Dr. Vladimir Chirvony is a Senior Researcher in the UMDO group at the ICMUV. His international experience includes a work in nanomaterial-related projects in the Institute of Physics (Minsk, Belarus), University Paris VI (France), Technical University of Valencia, and University of Valencia (Spain). He is the author of more than 120 research articles.

Dr. Rafael Ibáñez is an Associate Professor of Inorganic Chemistry at ICMUV since 1990.

B2.2.7. *ST Microelectronics (ST-i)*

Partner description and experience

ST Microelectronics is a broad supplier of semiconductors and subsystems operating on a worldwide basis in the merchant market. Its products cover a large range of all the major technologies from discrete components to complex digital signal processing systems. The company is world leader in analog ICs, mixed signal ICs, power ICs, MEMS, automotive, home entertainment, connectivity, microcontrollers and memories. The survey carried out by iSupply Corporation placed the company in rank N° 5 in the world market in 2009. The combined forces of ST Microelectronics come to over 51,000 employees (including ST-Ericsson), 10 R&D centers, 39 design centers, 15 production units, 78 sales offices in 36 countries.

Role in NAVOLCHI project

The ST Interconnect Systems Group (ISG) based it Catania, Sicily, is responsible for on-chip and off-chip interconnect systems development from architecture to Front-End implementation (gate level netlist), for both internal ST divisions and external customers. In this project the ISG group will be the project coordinator for WP6 (Integration, characterization and testing) and develop the CMOS circuits for the chip-to-chip communication modules, to be interfaced with the plasmonic interconnect devices. In addition, the ISG group will contribute to technical and economical evaluation forecasted in WP2 and

Key personnel contributing to the project

Alberto Scandurra is a senior silicon designer in the ISG group of ST. He received his degree in Electronic Engineering (Laurea) in 1997 from the Faculty of Engineering of the University of Messina (Italy). He has a wide experience in all the fields of SoC communication systems design, such as architecture, modeling, digital design; he gave a strong contribution to the development of the ST Network on Chip solution (STNoC) and is currently responsible for the activities related to chip to chip communication for Systems in Package applications. As member of the ST technical staff (a

restricted set of technical experts) he continuously works at the development of new concepts and architectures for on-chip and off-chip solutions, including novel technologies such as optical interconnect. According to that, he has been the responsible for ST for the WADIMOS European project.

B2.3. Consortium as a whole

B2.3.1. *Consortium overview and role of the participants*

The consortium constitutes of a group of legal entities that collectively hold all the required competence to achieve high quality results in accordance with the project objectives. To achieve the overall objectives within the project variety of challenges have been identified. Each of these objectives requires partners with an adequate background. The NAVOLCHI consortium optimally combines all the expertise necessary to carry out and achieve the ambitious goals and objectives of the NAVOLCHI project.

The NAVOLCHI objectives are aimed to the development of a new miniaturized Si-plasmonic technology well suited for the realization of miniaturized ultra-fast plasmonic interconnects which are factor of ten smaller than the current photonic counterparts.

These objectives are met with:

A consortium comprising of a balanced mix of industrial partners, research centers and a university partner:

- The industrial partner from the semiconductor device technology is ST Microelectronics.
- Three partners are from within research centers, i.e. IMEC, AIT.
- There are three university partners KIT, TUE, UVEG.

A consortium comprising people with a diverse background

- In physics (plasmonics, laser physics, nonlinear optics, integrated optics design, etc.)
- In semiconductor physics and chemistry (gain material preparation, deposition techniques, optical micro-spectroscopy, electro-optical characterization)
- In electrical engineering (design and fabrication of high speed electronics)
- In technology (CMOS silicon wafer fabrication, technology platform development)

A consortium comprising of partners that have devoted their recent years on the development of plasmonic both active and passive components that are necessary for realization of ultra-compact plasmonic receiver and transmitter. To complete the necessary expertise for the successful implementation of plasmonic interconnects, the consortium also includes legal entities that are well

familiar to the demand of the current and future electronic and Si-photonic markets. Combination of this two groups of parties will put the aggressively developing the field of plasmonics on the right track for fulfilling the requirements of the industry side

The Table below shows the needed competency and the partners that bring both the skill set and the equipment/facilities to perform the tasks covered within the work packages.

Skill set and Background	**Needed Competence**	**Partner**
System Architecture	System and Network Design, Value analysis and techno-economics	**AIT, ST Microelectronics**
Technology	CMOS fabrication technology	**IMEC, ST Microelectronics**
Laser physics	Plasmonic on-chip light source, III/V Technology	**TUE**
Plasmonics	Active plasmonics, Nano-fabrication	**KIT, TUE, UVEG, UGent**
Chemistry	Material research	**UVEG, IMEC**
CAD	Device modeling and CAD design	**KIT, IMEC, ST Microelectronics**
Optical communications	Device and System Testing	**ST Microelectronics, KIT**

A consortium comprising of partners with a strong interest in miniaturization of optical chip-to-chip interconnects and in demonstration of the dye-to-dye plasmonic prototypes:

- This is guaranteed by the participation of the device manufacturing company ST microelectronics that is one of the world leaders in providing the semiconductor solutions. ST microelectronics ensures that the direction of our focused research activities is well aligned with the expectations of the industry on the unique capabilities of plasmonics, therefore ensuring high impact of our project outcomes.

- KIT and in particular the Institute of Photonics and Quantum Electronics (IPQ) at KIT is known for bringing up new companies that work on disruptive technologies that have been developed in the course of research proposals. For instance, as of January 2009, the IPQ of KIT has founded a new start-up (Fibergy) that is based on a previous project.

B2.3.2. *Partners Expertise, Complementarities of participants*

The consortium composition has been carefully engineered in order to take into consideration a balanced effort allocation of months as per contributed work and as needed. We present here the corresponding distributions of MMs per partner and per country (see Figure 2.3.1).

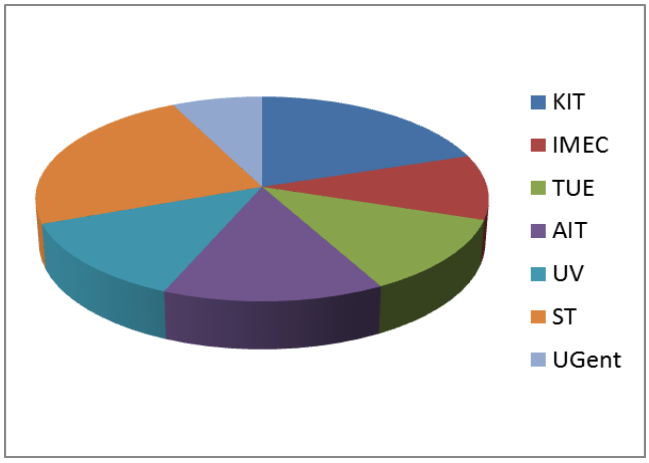


Figure 2.3.1 MM distribution among the partners

The partner's competencies are complementary and overlapping as can be derived from the Table in 2.3.1. They are complementary and cover all aspects needed to fulfil the project. In particular, we have silicon technology expertise from IMEC and ST Microelectronics, we have plasmonic expertise from TUE, KIT, UVEG, we have communications expertise from ST Microelectronics and KIT. The overlapping expertise is needed in order to mitigate the risk if one partner should have problems delivering.

B2.3.3. *Industrial involvement and exploitation of the results*

The NAVOLCHI consortium brings together five research groups across Europe and one industrial partner with strong activities on miniaturization of conventional optical interconnects via making use of plasmonics. These partners identify the NAVOLCHI vision being of critical importance to their future plans and interests. These partners consider the NAVOLCHI concept and particular the development of integrated plasmonics as an opportunity to be first and even to push the market. Other partners have a more focused approach and may use the project to gain knowledge and to develop pre-competitive product prototypes.

The exploitations plans are presented in detail in section 3

B2.3.4. *Subcontracting*

UVEG would subcontract the spin-off company (micro-SME) Intenanomat SL promoted by the research group for preparation of composite nanomaterial (see technical description of the different materials in section 1.3.1.2), as the base for developing SPP waveguides, gain layers/stripes and photodetectors. Intenanomat owns a microplotter for subpicoliter dispensing of QD-inks and QD-polymers with a spatial resolution of 5 micron, in order to define dots and stripes (minimum width of

5 micron) to be used by the UVEG group in experiments with gain layers and photodetectors, as, a simpler alternative to UV photo-lithography (available at the UVEG group)[63].

This subcontract is mainly substanced because the know-how of the UVEG group with the chemistry of composite nanomaterials (base of materials and procedures listed in 2.4.2) was developed between 2007 and 2010 by Dr. Abargues, who (now is R&D manager in Intenanomat, spin-off company of the UVEG group). The company was founded as a spin-off of the university of Valencia by agreement of its council since July 2010. For these reasons the subcontract was suggested to be awarded to Intenanomat and no to other companies (we do not know other having this know-how). Furthermore, the amount of the subcontract is very reduced, with a cost equivalent to less than 9PM of the project or, simply, the equivalent to the costs of the needed chemical consumables (polymers, reagents/reactives, gases, other lab consumables) and use of microplotter and other equipment. Take into account that the UVEG group has not included any chemical cost in the R+D budget.

B2.3.5. *Other countries*

No non-EU parties are included in the NAVOLCHI project.

[63] NOTE: Other than chemical synthesis work developed by the subcontractor, the UVEG group possibly will hired a postdoc (chemistry/physicochemistry) in the present project during one year, approximately, that will optimize the materials listed in 2.4.2 and he will be responsible to prepare, characterize and optimize QD-based solutions and photoconductive layers by different methods (layer-by-layer method, for example). All the chemistry reactive and some chemistry equipment (centrifuge, not available at the group) will be serviced by Intenanomat.

B2.4. Resources to be committed

B2.4.1. *Available equipment*

The major resources that each partner will provide and the relevance to work plan is given in the table below:

Test bed/ Equipment	**Software tool /Algorithms**	**Relevance to WPs**
KIT		
– Fully equipped cleanroom facilities equipped with E-Beam lithography, metallization, CVD, dry- and wet-etching tools, Focused Ion Beam – Integrated optics / silicon photonics characterization setup: Linear and nonlinear optical measurements, electrical characterization < 100 GHz – C-band testbed: 300 km recirculating dispersion compensated loop – Transmitter: Software Defined 336 Gbit/s transmitter for all modulation formats up to 28 GBaud/s, 10 and 40 GBit/s RZ/NRZ/DPSK, 80, 120 and 160 Gbit/s OTDM, 42.7 GBd/s QPSK – Receiver: Coherent receiver for up to 40 GSamples/s – Modulation Analyzer – Optical test equipment: 10 and 40 Gbit/s BERT set, FROG measurement setup, 70GHz sampling oscilloscope with 70GHz photodiodes, OSAs, Lightwave component analyzer, Polarization analyzer, Pump probe setup – Electrical test equipment: 65 and 110 GHz network analyzer, 50 GHz spectrum analyzer,	– Component simulation: Rsoft Fullwave/Beamprop/Femsim, CST Microwave Studio, Ansoft HFSS – COMSOL Multiphysics – System simulation: RSoft Optsim – Matlab / Simulink	WP3 WP4 WP5

50 GHz synthesizer, 50 GHz coplanar probes		
TUE		
– III-V cleanroom facilities which include among others the following equipment: – Electron Beam Lithography (Raith 150 II) – Optical contact lithography (Karl Suss) – ASML deep UV scanner (90nm resolution) – ICP RIE (Oxford Instruments) for InP – PECVD (Oxford Instruments) for dielectric deposition – Electron Beam Evaporation, Thermal evaporation, Sputter, for deposition of many different metals. – Rapid thermal annealing – Wet chemical processing facilities	– Custom FDTD code for simulation of plasmonic devices – Lumerical FDTD software	WP3
IMEC		
– High-resolution lithography based on 193nm lithography on 200mm wafers for fabrication of nanophotonic waveguides – Processing technology and experience with new materials on silicon photonics (including nanostructuring). . – Optical measurement infrastructure for static and low-speed measurements (up to 10Gbps	– IPKISS/PICAZZO: waveguide circuit design tools, including large libraries of passive functional components. – CAMFR (on cluster): eigenmode solver – MIT's MEEP (on cluster): FDTD Maxwell solver. – Photon Design: Fimmwave, Fimmprop3D, Kallistos, Omnisim, Crystalwave – Phoenix BV: Optodesigner, Flowdesigner – ASPIC: circuit simulation	WP3 WP4 WP5

	– DIOS, Dessis, TCad – Comsol: multiphysics – Matlab	
UGent		
– Fully equipped nanoparticle synthesis lab. – Quantum dot post-processing facilities – ligand exchange, embedding in inorganic matrices. – Structural and morphological characterization equipment (XRD, TEM, SEM, …) – Steady state and time resolved photoluminescence setup		WP4
AIT		
– Test equipment: 10Gbit/s BERT set, OSA, 40Gbit/s Communications analyzer. – 160Gb/s transmission capabilities with 10GHz Mode Locked laser and OTDM – Various components (mode-locked lasers, passive elements, filters, amplifiers, etc.) – Recirculating loop supporting 80 channels C-band 50 GHz channel spacing, with 5 amplifier spans and a variety of fibre types (SMF, LEAF, Truewave and corresponding dispersion maps).	– Modelling of transmission impairments in Matlab – System performance evaluation using VPI	WP2 WP5 WP6
UVEG		
– Ebeam + UV lithography + spinning + chemical bench + metal coating (sputtering, evaporation) – Dry + wet Si-oxidation o Si wafers by using RTP (Rapid Thermal Processing) to develop organic photonic devices. – Basic electrical/Electrooptical characterization	– FDTD (Microwave Studio), COMSOL. – Genetic algorithm + 2D Multiple scattering theory for inverse design. – Effective mass models for optical transitions in	WP4

of materials-photoconductors-photodiodes. – Confocal optical micro-spectroscopy setup for single quantum dot Photoluminescence, temperature range 4 – 300 K, wavelength detection range 400-1700 nm, tunable lasers 700-1000nm (and pulsed) + 1470-1550nm, pulsed lasers at 830 and 980 nm. – Standard optical spectroscopy setups single channel and multichannel + photoluminescence (including time resolved) in different ranges (VIS+NIR). – Optical setup for characterization of nanostructured single-/multi- layer structures and nanophotonic structures/devices: inverted microscope, optical multichannel fiber optic minispectrometers (VIS and NIR), UV-VIS reflectometer. – Institute/campus facilities SEM, TEM, AFM, FTIR for structural/morphological characterization of materials and devices.	Quantum dots.	
ST-i		
– FPGA boards, high speed-characterization setups, network analyzers all necessary equipment to characterize interconnects	– Functional verification: Incisive (Cadence) – FE synthesis: Design Compiler (Synopsys) – BE-driven synthesis: Design Compiler Topographycal (Synopsys) – Formal verification: Formality (Synopsys) – DFT: Teramax (Synopsys) – Design qualification: Spyglass (Atrenta)	WP6

B2.4.2. *Explanation of cost details*

The resources described in the previous subsections are committed will be accessible by all contributing partners that offer their services towards the completion of the NAVOLCHI project's objectives. Where possible and if required, individual resources will be shared among users exclusively for the completion of the project's objectives.

In the following section we represent an explanation for the direct costs required by each of the participants. We present a direct cost distribution among the work packages and their deliverables. In addition, we break down the direct cost of each work package among the equipments, chemicals, software license fees etc..

KIT			
WP	Deliverable	Cost	Equipment/ Facility available
WP1	D1.1 D1.2 D1.3 D1.4 IPR D1.5 IPR		In support of the coordinator activity, KIT has access to: State-of-the art online communication tools for teleconferencing, latest web dissemination software tools and facilities. The Institute of Photonics and Quantum Electronics from KIT has a full-time employed network administrator and three secretaries that can support the administrative part of the project. KIT also has a university employed legally authorized officer to support European projects.
WP2	D2.2	2k€	Partial Contribution to RSoft photonics lincense
WP3	D3.2	3k€	Partial Contribution to RSoft photonics lincense
	D3.4	5 k€ 5 k€ 17 k€	Silicon on insulator wafers Mask for UV lithography Flexure Stages with their piezo controllers, as well as high quality lense PM fibers, polarization controllers, polarization beam splitter
WP4	D4.5	6 k€	Maintenance fee for software for 3 years, Depreciation on 1 computer
WP5	D5.5	7.62 k€	Chemicals, mask for UV lithography as well as crucibles for metal evaporation

WP6	D6.1 D6.2	12 k€	Due to the ultra-compact dimensions of the plasmonic modulators high speed RF prober station with ultra-compact pitch is required: 10 k€
WP7	D7.1, D7.2, D7.4, D7.5, D7.7	20k€	Travel expenses
	Subcontracting	2k€	Certificate on the financial statements
		2k€	Total sum (Subcontracting)
		77.62k€	Total sum (other direct cost)

IMEC			
WP	Deliverable	Cost	Equipment/ Facility available
WP3	D3.3, D3.4	2k€	To purchase wafer bonding materials on SOI structure
WP4	D4.1, D4.4	5 k€	SOI wafers and maskplates
WP5	D5.3, D5.5, D5.7	3.35 k€	SOI wafers and maskplates
WP7	D7.1, D7.2, D7.4, D7.5, D7.7	15k€	Travel expenses
	Subcontracting	4.4k€	Certificate on the financial statements
		4,4k€	Total sum (Subcontracting)
		25.35k€	Total sum (Other direct cost)

UGent			
WP	Deliverable	Cost	Equipment/ Facility available
WP4	D4.1, D4.4	12 k€ 9 k€	Chemicals, gases, running costs synthesis lab Structural characterization (XRD, TEM)
WP7	D7.1, D7.2, D7.4, D7.5, D7.7	5.6 k€	Travel expenses
		26.6k€	Total sum

TUE

WP	Deliverable	Cost	Equipment/ Facility available
WP2	D2.2, D2.6	2 k€	Partial Contribution to Software
WP3	D3.1, D3.3	45.65k€ 6 k€	Cleanroom fee for PhD students (5k€ anually) Epitaxially grown InP/InGaAs wafers
WP7	D7.1, D7.2, D7.4, D7.5, D7.7	10 k€	Travel expenses
		63.65k€	Total sum

AIT			
WP	Deliverable	Cost	Equipment/ Facility available
WP2	D2.2, D2.3, D2.5, D2.6	6 k€	2 VPIphotonics licenses for for 2 years
WP4	D4.1, D4.2	4 k€	1 VPIphotonics license for for 1.5 years and 1 optsim lincense for 1 year
WP6	D6.4,	12 k€	Optical and electronic consumables for the support of test-bed that will be used in the test and measurement activities described
WP7	D7.1, D7.2, D7.4, D7.5, D7.7	20 k€	Travel expenses
		42 k€	Total sum

UVEG			
WP	Deliverable	Cost	Equipment/ Facility available
WP4	D4.2, D4.4, D4.5,	40k€	The contribution envisaged for our spin-off company "Intenanomat SL" will include materials to be prepared or developed and furnished to the UVEG team: Colloidal silver or gold nanowires 100-200 nm in diameter and 10 micron long (for 1D waveguides based on metal nanorods). Lithographic (dielectric) resists doped with QDs for patterning of cladding materials for plasmon amplification. PVA e-beam litographic resist with Au-nanoparticle precursor (alternative fabrication technique for 1D waveguides by using nanocomposites and regrowth after patterning). Electrical conducting lithographic resist (+ gold nanoparticle precursor) to perform micropatterns for plasmonic photoconductors. Developing a layer-by-layer method to obtain photoconductive layers of QDs (base of nanogap photoconductors/photodetectors and LEDs). Development of solutions made of conductive polymer and QDs capped with short chain ligands.
	D4.1, D4.2, D4.3,	10.500k€ 5 k€ 6 k€ 2.5k€ 6 k€	Maintenance of cleanroom facilities: UV and Ebeam facilities, spin-coating, metal coater, profilometer and AFM (3500€ per year) 2 objectives high NA optimized for NIR Precision piezoelectric XYZ translator () Ectrical characterization of photoconductors: pA current source Keithley-quality (to be co-funded): Infrared camera (for observing light coupling into plasmonic structures, detectors and devices), to be co-funded
WP6	D6.1	7 k€	General optics/optomechanics and electronics/informatics (i.e. maintenance of minor elments for optical setups): 2 k€ per year

WP7	D7.1, D7.2, D7.4, D7.5, D7.7	18 k€	Travel expenses
		40 k€	Total sum (Subcontracting)
		55 k€	Total sum (Other direct costs)

ST			
WP	Deliverable	Cost	Equipment/ Facility available
WP2	D2.1, D2.4	7 k€	CADENCE simulator lincense
WP5	D5.1, D5.2, D5.4, D5.6	39.2 k€	Synonpsys / Cadence design tools lincenses
	Subcontracting	2 k€	Certificate on the financial statements
		2 k€	Total Sum (Subcontracting)
		46.2 k€	Total sum (Other direct cost)

Distribution of Human Resources of each partner over the WPs and the respective tasks

WP	Partner							Task
	KIT	IMEC	UGent	TUE	AIT	UVEG	ST	
WP1	8	0.5	–	1	1	0.75	1	Task 1.1
	8	0.5	–	–	1	0.25	1	Task 1.2
WP2		–	–	–	3	–	4	Task 2.1
	1	0.25	–	2	9	1	0.5	Task 2.2
	0.5	0.25	–	2	3	0.5	0.5	Task 2.3
	0.5	0.5	–	2	3	0.5	1	Task 2.4
	–	–	–	–	–	–	6	Task 2.5
WP3	–	1	–	5	–	–	0.25	Task 3.1
	6	–	–	–	–	–	0.25	Task 3.2
	–	1	–	24	–	–	0.25	Task 3.3
	20	1	–	–	–	–	0.25	Task 3.4
WP4	–	–	–	–	9	2	0.2	Task 4.1
	1	3	–	–	–	4	0.2	Task 4.2
	–	–	24	–	–	3	0.2	Task 4.3
	–	7	–	–	–	7	0.2	Task 4.4
	2	1	–	–	–	16	0.2	Task 4.5
WP5	8	2	–	–	–	4		Task 5.1
	–	5	–	–	–	–	–	Task 5.2
	2	7	–	–	–	–	–	Task 5.3
	1	–	–	–	–	–	28	Task 5.4
	1	–	–	–	–	–	2	Task 5.5
WP6	2	3	–	3	5	1	–	Task 6.1
	1	–	–	–	–	1	2	Task 6.2
	1	–	–	–	2	–	2	Task 6.3
	–	–	–	–	3	–	18	Task 6.4
WP7	1	0.5	–	0.3	4	1	4	Task 7. 1
	1	0.5	–	0.3	1	–	2	Task 7.2
	1	–	–	0.4	3	–	4	Task 7.3

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B3. IMPACT

B3.1. Strategic impact

NAVOLCHI focuses on the development of innovative metal-silicon-organic hybrid lasers which is not currently available. The developed NAVOLCHI technologies will enable a paradigm shift in the functionality towards realization of next generation single photonic integrated microchip with all needed photonic components that would consume less energy and low cost high volume manufacturing capabilities.

NAVOLCHI enables energy efficient solution for light emission. The innovative laser targeted in this project for example plasmonic laser would require a very low threshold current in the range of sub mA or 1-2 mA for stimulated light emission, which is a factor 10 times lower than any other efficient lasers (i.e. DFB, DBR, SGDBR) reported so far. This would provide a much Greener solution by reducing energy consumption at the transceivers more than 5-10%.

NAVOLCHI enables optical interconnection networks in advanced computing and network systems. Leading researchers companies and academia expect that integrated photonics will dominate in advanced computing and network systems.[64] The *trend for optical interconnects in computing systems* is a transition of from present-day rack-to-rack connections to connecting boards via an optical back-plane, and to extend the technology to allow even on-board optical PICs modules capable of connecting multiple cores on digital ICs. The final goal will be the ultra small and compact on-chip optical interconnect at Tbit/s-rates for realizing an optically connected three-dimensional layer stacking of processors, memories and any other Intellectual Properties such as audio/video coprocessors, DMA engines, application processors for multimedia, RF modules etc. (System in Package, SiP) in photonic network interconnect plane to realise supercomputer chip, an industry vision for the year 2018 that might be realized with an approach such as NAVOLCHI..

NAVOLCHI enables new functionality in medical appliances and sensing applications. NAVOLCHI will make new functionalities available that are not supported by silicon alone or by organic materials that will be added in a backend processing step. This is the case of the polymer based composites, containing metal nanoparticles and II-VI or IV-VI quantum dots, for which Localized Surface Plasmon Resonance and fluorescence, respectively, are the optical signals to be used for transuding. Furthermore, NAVOLCHI propose the development of these nanoparticles embedded in patternable matrices, which enables the direct fabrication of biochips in a single step and low cost.

Plasmonic lasers will outperform other microlasers, the most promising ones being Photonic Crystal lasers. Whereas power dissipations of plasmonic lasers and photonic crystal lasers may be comparable, plasmonic lasers will be much faster due to the much smaller volume of their laser cavity and their active region. Their low power and high speed will allow them to be integrated in ultrafast

[64] Y. Vlasov (IBM), K. Bergman (Columbia), A. Krishnamoorthy (Sun): Can integrated photonics enable optical interconnection networks in advanced computing and network systems? OFC 2009. Workshop OSuE

processor cores in electronic processors. In this way they could extend the validity of Moore's law with one or two decades. Ultimately they might appear in each laptop which would provide them with a huge economic impact. All of this is very speculative, at present, but plasmon lasers clearly have the potential to cause a major breakthrough in the application of photonics.

Plasmonic modulators developed by NAVOLCHI will outperform the state of the art solutions in terms of its footprint, speed, power consumption as well as ease of integrability on electronic circuits. They will be 1-20 μm in length and will operate with a 1.5 V voltage swing. Modulation speed of these modulators will reach 100Gbit/s and beyond. Such attractive properties of them will pave the way to a new generation of high speed compact opto-electronic chips with advanced functionalities such as routing, switching, multiplexing, wavelength conversion etc.

Plasmonic polymer based photodetectors have small footprints and can be fabricated on CMOS technology. The versatility of the proposed photodetectors is ensured by many material parameters, device geometry and configuration that can be varied. This is useful not only for development of transceivers for on-chip and inter-chip communication, but also for integrated optical/electrical lab-on-a-chip sensors using CMOS technology platform in chemical/biological/medical applications.

Plasmonic amplifiers: currently amplifiers on the silicon platform are either based on Raman gain or on III-V hybrid integration using wafer-bonding techniques. The NAVOLCHI amplifiers based on colloidal quantum dots will outperform those amplifiers in terms of size (compared to Raman and hybrid), power consumption (compared to Raman) and ease of integration (compared to hybrid). In addition, novel types of quantum dots will be developed having improved gain characteristics and possibly compatible with direct current injection. This will not only have impact on optical amplifiers but also lasers integrated on the silicon platform.

B3.1.1. *NAVOLCHI Relevance with expected Impacts Listed in Work Programme*

NAVOLCHI focuses on meeting the prime goals and expected impacts of the objective **ICT-2011.3.5 Core and Disruptive Photonic Technologies** of the FP7 work programme. NAVOLCHI addresses application-driven research with a view to industrialization, where priority is given to a break-through approach that represents a disruptive new technology. The following discussion elaborates the ways in which the NAVOLCHI concept meets the expected impacts.

Expected Impact 1: Long-term potential of European industrial leadership in integrated

Higher capacity in optical transmission systems requires small footprint, high speed and power efficient transmitter and receiver best suited not only for long but also short distance communication as for chip-to-chip interconnects. Si-plasmonics offers an advanced platform for robust, highly-integrated devices that are able to guide and strongly confine near-infrared light. Additionally, making use of III-IV semiconductors and organic polymers as active materials the passive plasmonic waveguides can be activated for their application as ultra-compact **light sources, modulators and photodetectors** that are of key importance for chip-to-chip interconnects.

NAVOLCHI provides technology solutions for *both communication and computer hardware industries.*

NAVOLCHI developed interconnects will achieve p*ower consumption* significantly lower than the competing technologies due to the combination of quantum effect in ultra small plasmonic components and Si waveguides. .

The nanoscale NAVOLCHI *switching elements* dramatically increase the effective port count and data transfer rate for optical interconnects. As a matter of the fact, the NAVOLCHIs photonic devices will have dimensions so far only seen in electronics so that higher integration levels would be feasible.

NAVOLCHI approach is based on CMOS compatible processes, with its *ease of manufacturing complexities, high yields and reliability* over existing technologies. This technology is more practical and has good chance to go into products.

NAVOLCHI opens the road to to a *co-integration of electronic circuits and plasmonic devices* of similar dimensions on the same silicon chip, which doesn't exist currently.

NAVOLCHI is considered to be a promising solution by an Eureopean industrial leader (ST Microelectronics). ST not only supports the NAVOLCHI proposal but also will be strongly working towards securing IP and evaluation of the solution for their future comercial products and so as for the business growth for the ST Microelectronics.

The NAVOLCHI solution will lead to new applications in the related markets. The project's focus is on the chip-to-chip interconnect market. Yet, the idea and concepts have wider applications. The availability of cheap miniaturized transmitters and detectors on a single chip will enable new applications in sensing, biomedical testing and many other fields where masses of lasers and detectors are needed to analyze samples in hospitals.

NAVOLCHI is is the only viable approach for a massive monolithic integration of optoelectronic functions on Si substrates as it relies to the most part on the standardized processes offered by the silicon industry. Thus, it has a long term economic potential.

Expected Impact 2: Securing European industrial leadership and market share

NAVOLCHI will contribute to the continued European RTD leadership in integrated plasmonics by addressing the growing trend towards advanced electro-plasmonic devices, with enhanced properties in footprint, bit-rate as well as in energy consumption. The participation of a major company like ST in our consortium ensures the implementation of this expected impact. In addition, all research centres and universities.

B3.1.2. *Key ICT challenges of FP7 framework addressed by NAVOLCHI*

NAVOLCHI addresses key ICT objectives of the FP7 framework. Specifically NAVOLCHI aims to:

Strengthen Europe's scientific and technology base and improve the long term competitiveness of European industry in the globe.

For many years, **plasmonics** have been considered as a solution for high speed deep miniaturized integrated optics which is capable of manipulating the light in the dimensions comparable to electronics. NAVOLCHI makes use of plasmonics in order *to miniaturize the high speed photonics* for its application as *small footprint optical chip-to-chip interconnects*. The ideas

covered within the NAVOLCHI will lead to the *increased performance in electronics and silicon photonics and most likely having its impact on the market within 10 years*. Ultra-small size of the plasmonic devices proposed by NAVOLCHI paves the way to large scale integrated plasmonics manufactured in parallel to electronics which can serve as a key for the development of future *ultra-fast multi-core computing systems*. Thus, making use of Si-plasmonics platform for high speed chip-to chip interconnection, NAVOLCHI meets the ICT objectives of "*miniaturization, large scale integrated functionalities, multi-core architecture*" as well as shows a strong potential of improving energy efficiency due to the strong field confinement in active regions of the lasers and modulators. The plasmonic chip-to-chip interconnection architecture proposed by NAVOLCHI provides reduced complexity and efficient utilization of resources, which in turn allows for significantly reduced CAPEX and OPEX.

Help to drive and to stimulate products as well as feed innovation

The NAVOLCHI consortium includes a strong technological partner: ST Microelectronics that will be actively involved in the design and commercialization of the developed plasmonic interconnects. The major role of the ST Microelectronics is to assist in the design and fabrication of the NAVOLCHI devices by applying industrially compatible fabrication technology and thus ensure the commercial exploitation of the NAVOLCHI technology. Furthermore, the outcome from each stage of the project will be conveyed to the ST Microelectronics so as to feed innovation from the universities and the industrial partners towards them. The ST Microelectronics will ultimately combine the generated know-how with their expertise in order to develop commercial products and thus contribute to the exploitation of the NAVOLCHI technology. Moreover, participation in the project will offer ST Microelectronics the opportunity to build strategic partnerships, to extend their know-how and to expand their market with higher value innovative projects.

High risks in Plasmonics

The unavoidable plasmonic losses from metals make the commercialization of the plasmonic devices challenging in spite of their attractive properties. Gaining maximum benefits from these plasmonic devices can be achieved by their more aggressive downscaling which boosts the optical field confinement in the active region of the devices. However, such an aggressive downscaling usually rise to several issues concerning the device fabrication as well as the performance of the device itself. The risks are followings:

For the correct functionality of the plasmonic transmitter and receiver, the accurate alignment of the components composing the latter should be guaranteed. The required alignment accuracy – limited by fabrication tolerance – obviously increases with reducing the footprint of each individual component.

Well known properties of the materials composing the individual device might deviate from their bulk properties due to the *low-dimensional characteristics* which itself might result in unexpected device performances.

B3.1.3. *Impact on the competitiveness of the proposers*

B3.1.3.1. Direct applications and market prospects

NAVOLCHI will enable high performance, low power System in Package technology with advanced chip-to-chip interconnect physical layer thanks to the plasmonics-based emitters and detectors.

According to the technology and products trend ST is moving its focus from System on Chip (SoC) to System in Package (SiP) and a reliable, high performance, low power interconnect system allowing multiple dice to communicate to each other is mandatory.

Thanks to this novel approach ST will be able to play a key role in the market of a variety of consumer applications, ranging from Set Top Box to automotive, computer, TV, mobile phones and more.

The expected impact of the NAVOLCHI in terms of industrial application and market prospects can be summarized in the following points:

Allow European companies such as ST, and ST Interconnect Systems Group in particular, to master new communication architectures and technologies for SiP approach and bring/keep the company in a world-leading position.

Contribute to the widespread integration of high performance, efficient and reliable communication solutions in products.

B3.1.3.2. Improve Europe's position in systems communication architectures, in particular in SiP contextPotentially patentable ideas

NAVOLCHI project is driven by several ideas that are potentially patentable that can serve as solution to high speed and power efficient communication:

- Plasmonic Nano-Laser
- Surface Plasmon Polariton Absorption Modulator (SPPAM)
- Surface Plasmon Polariton Electro-optic Mach-Zehnder Modulator (SPPMZM)
- Plasmonic patternable polymer based photodetectors
- Hybrid-silicon plasmonic optical amplifier based on colloidal quantum dots
- Plasmonic Chip-to-Chip interconnection architecture
- Die to die communication module architecture and micro-architecture
- Encoding techniques for low power transmission over die to die physical link
- Encoding techniques for error detection and correction over die to die physical link

B3.1.3.3. Benefits and competitive advantages

NAVOLCHI aims to design and fabricate a fully functional plasmonic transmitter and receiver with an on-chip light source for chip-to-chip interconnection. Employing the on-chip plasmonic nano-scale light source and compact plasmonic modulators, the dimension of proposed transmitter is reduced down to several square micrometers. NAVOLCHI focuses on two distinct plasmonic modulator approaches – surface plasmon polariton absorption modulator and electro-optic Mach-Zehnder modulators. The operating speeds in such modulators exceed 100Gbit/s, due to the high carrier mobility in the highly conductive metal-oxide and the instantaneous linear-electro optic effect in organic polymers. Moreover, as a contingency plan, NAVOLCHI also considers a possibility of a direct modulation of the plasmonic nano-laser, whose ultra-small capacitance defines its RC-limited operating speed above 100Gbit/s. NAVOLCHI will also model and fabricate the plasmonic receiver with a high performance and an ultra-compact dimension. To reduce the overall optical losses in metals, NAVOLCHI will develop a plasmonic amplifier with a positive net-gain. The practicability of the amplifier for its integration for chip-to-chip interconnection is guaranteed. To avoid unbeneficial additional plasmonic losses, NAVOLCHI makes use of low loss passive silicon components as simple waveguides and filters. By using the developed plasmonic interconnects technology will minimizes the pin and power overhead of chip-to-chip interconnects and provides a scalable solution that can be used throughout an entire system. The interconnect technology is very scalable solution with the capability of operating over a variable number of processor-lanes with no inherent limit on the data rate per interconnect link.

B3.1.3.4. Economic justification

Information and computing technology is one of the significant employment and economic sectors of Europe. NAVOLCHI will help foster innovation is this sector over a wide geographical area of Europe. Ultimately such nano-scale transmission systems as proposed here could become part of every PC or high performance computing device. As such there will be a widespread and profound economic impact.

B3.1.4. *Strategy for impact achievement*

The inclusion of the commercial partner ST Microelectronics will provide a vehicle with which the technology can be exploited for use in products. The strategy that will be followed for achieving the industrial impact will consist of promoting the chip to chip interconnect developed during the NAVOLCHI project execution phase between ST internal divisions and external customers relying on SiP approach for the development of their products. Results of benchmarking activities will be a key to convince potential customers to embrace the novel proposed solution.

Furthermore, via integrated optics technology and design courses held at the academic consortium partners, the concepts and technology developed in NAVOLCHI can be passed on to many other new scientists/engineers, throughout Europe.

B3.1.5. *European dimension*

The knowledge, expertise, and technology to be developed in NAVOLCHI are leading edge. Technical skills and competences are not present in one country hence we have composed a pan European consortium that will provide extensive, complimentary competencies, resources and facilities. Each of the participants represents State of the Art in their field or has extensive competence within the technology they are contributing in the project.

B3.1.5.1. Improvement of European social and economic cohesion

NAVOLCHI will bring together students and workers from southern, central and northern Europe. Furthermore, the results of NAVOLCHI are to improve among other things the quality of information and communication technologies. These technologies which make up the internet are crucial to reducing barriers to information and services and thus act as a leveller in society.

B3.1.5.2. Employment

The NAVOLCHI technologies is crucial to the continuous roll-out of new products needed to compete internationally with a long-term approach in addressing key elements for future innovation in industries with a large job-creation potential, primarily in the super speed multi-core PCs, data centres, and faster memory access links. The developed technology in the NAVOLCHI has potential capability to offspring small and medium-sized enterprises (SMEs) that can be ranked as pure photonic businesses at nano scale in Europe. These innovative SMEs can occupy a distinct segment in the value-added chain and make an important contribution to know-how transfer from research to industry. SMEs consequently serve a key function in most high-technology fields, and establishing innovative start-ups is therefore of enormous importance in the young plasmonic photonic industry and to create the jobs of the future by applying NAVOLCHI technologies with ideas for innovative products and services.

B3.1.5.3. Environment

The ICT industry has a very significant role to play in reducing greenhouse gas emissions. In 2007, the total footprint of the ICT sector – including personal computers (PCs) and peripherals, telecoms networks, processors and devices – was 830 MtCO2e, about 2% of the estimated total emissions from human activity released that year. The carbon generated from materials and manufacture is about one quarter of the overall ICT footprint, the rest coming from its use. Currently, Data centres account for 14% of the total greenhouse gases emissions, and it is expected to grow to 18% by 2020 [[65]]. Despite first-generation virtualisation and other efficiency measures, data centres will grow faster than any other ICT technology, driven by the need for storage, computing and other

[65] SMART 2020: Enabling the low carbon economy in the information age, The climate group, 2009

information technology (IT) services. Therefore, it is extremely important for Europe to focus on the research of more energy efficient datacenters that will reduce the percentage of emissions.

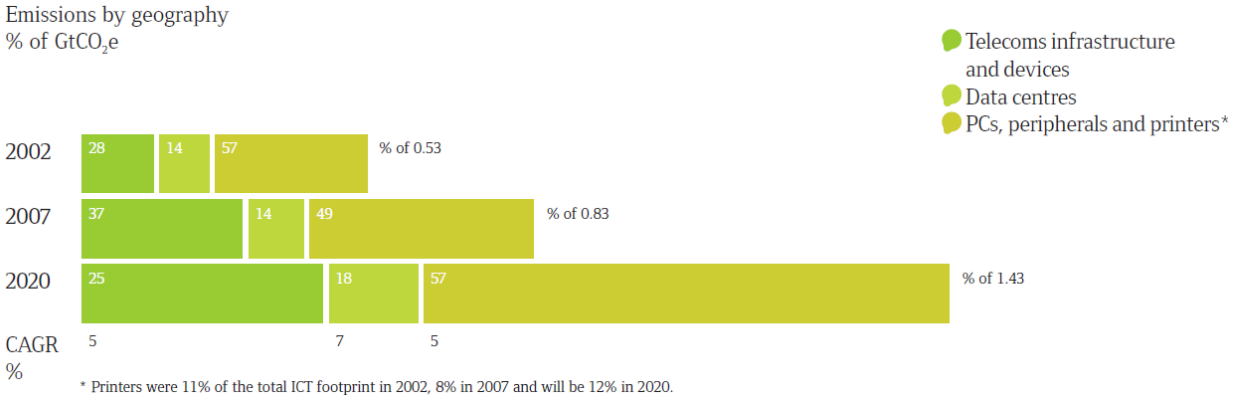

Figure 3.1.1 According to the same study, In 2002, the global data centre footprint, including equipment use and embodied carbon, was 76 MtCO2e and this is expected to more than triple by 2020 to 259 MtCO2e – making it the fastest-growing contributor to the ICT sector's carbon footprint, at 7% pa in relative terms.

Figure 3.1.2 The Global data centre footprint, Source: Smart2020 [65]

B3.1.6. *Other relevant European or Nationally funded research*

The following list reviews international corporations and activities in the field of integrated plasmonics. Yet, these approaches do not provide a fully functional transmitter and receiver consisting of light source, modulators, amplifiers and photodetectors and are not applicable for electrical die-to-die interconnection.

Currently there are several STREPs in the field of plasmonics that are driven by EU under the FP7.

- *Platon:* http://www.ict-platon.eu/
  The project focuses on a dielectric loaded surface plasmon polariton waveguides and thermo-optic switches for realization of optical routing fabrics for optical interconnects. However, the slow thermo-optic effect as well as absence of an on-chip light source makes Platon's vision not applicable for die-to-die interconnection.

- *Active Plasmonics:* http://www.activeplasmonics.org
  The project focuses on both passive and active plasmonic components. To achieve signal switching, modulation, amplification and detection the project proposes a hybridisation of plasmonic nanostructures with functional (molecular or ferroelectric) materials. However, the main focus is on the optically controlled switches and the vision does not include on chip light source.

- *PLAISIR:* http://www.plaisir-project.eu
  The objective of the PLAISIR project is to transpose the latest advances in plasmonics achieved in the visible to the mid-IR, where the potential for devices can impact two key areas: spectroscopic chemical sensing and mid-IR photodetectors.

In an *international* level, the consortium of NAVOLCHI project has taken into account the major relevant research activities, has considered their solutions and has assessed their limitations. Exploitation of previous research activities is ensured in NAVOLCHI as its partners have been actively involved in related projects and are bound to extend their work under the umbrella of NAVOLCHI objectives. NAVOLCHI partners are involved in other international projects which are related to photonic components under FP6 and FP7, and they have already gained significant know-how in the fabrication and exploitation of partially organic photonics or CMOS-technology. For instance, KIT has recently served as coordinator of the EU-project **TRIUMPH, SOFI**, and IMEC has served as project manager for the project **ePIXNet** (*Photonic integrated components and circuits - IST*).

B3.2. Plan for the use and dissemination of foreground

Dissemination of ideas and results has high importance in the NAVOLCHI project. In order to make the NAVOLCHI vision to become a reality in the future, information about the proposed changes must be brought out to the research community and the decision-making actors in the market. Dissemination of project results is organised directly under WP7. The dissemination plan described in chapter 3.2.1 will be reviewed during the first 6 months of the project. This plan will contain concrete goals for dissemination that will oblige each individual partner to certain activities and actions. The PM has the overall responsibility for dissemination, while the WP7 leader has the day-to-day responsibility of following up this plan, which will be continuously updated during the whole life-time of the project.

B3.2.1. *Detailed dissemination activities*

The partners of NAVOLCHI are top research organizations with proven track record in their field are very active in disseminating their research results in a worldwide range to scientist, to industry and to the public.

B3.2.1.1. Scientific dissemination activities

Scientific Journal Publications (Task 7.1)

Scientific dissemination of the NAVOLCHI results will be obtained through contributed and invited papers in top refereed scientific journals. Specifically NAVOLCHI partners will publish their work in journals of the IEEE, the Optical Society of America and Elsevier Optics Communications.

Technical Conferences (Task 7.1)

NAVOLCHI research results will be disseminated through technical presentations in prestigious international conferences and workshops. Given the track record of the NAVOLCHI partners in regular, invited and post-deadline contributions, NAVOLCHI is expected to have a strong impact on the following leading conferences such as the European Conference on Optical Communication, Optical Fiber Communication Conference, Conference on Lasers and Electro Optics Europe. Moreover, the NAVOLCHI consortium will actively pursue to organize workshops in new member states of the EU and participate in local meetings hosted in the aforementioned countries.

From systems point of view NAVOLCHI project results will be presented at various international conferences focused on Systems on Chip (SoCs) and Systems in Package (SiPs) in terms of both technology and methodology, such as DATE, SoC, IP-SoC and others.

Scientific magazines (Task 7.1)

NAVOLCHI members will publish articles containing breakthrough results with simplified technical content in printed or online magazines like Laser Focus World, Europhotonics and Photonics Spectrum.

Organization of summer school (Task 7.3, Deliverable D7.7)

NAVOLCHI members will organize a summer school for young researchers, PhD students as well as employees from companies investing knowledge in future optical networking technologies. The purpose of the school will be to convey expertise gained through the project towards all the partners and to extend the scientific skills of the participants.

Advertising the Technology Platform (Task 7.1, Deliverable D7.6, Deliverable D7.7)

Upon successful completion of the project the realization of a technology platform is envisaged. This will serve as a means of dissemination since it will contain the know-how that the consortium has developed regarding silicon-organic hybrid photonics in order to use them in innovative products.

B3.2.1.2. Exhibitions dissemination activities

NAVOLCHI project will be represented in booths at major exhibitions through the SME partners of the consortium (Task 7.1, Deliverable D7.1, and D7.4). These exhibitions take place during the biggest and most prestigious conferences in the optical communication area in Europe and the United States, including the ECOC, CLEO Europe and Optical OFC. These booths are expected to generate commercial interest for NAVOLCHI technology through interaction with system vendors and academic researchers.

B3.2.1.3. General Public dissemination activities transfer

Public Events (Task 7.1, Deliverable D7.1, D7.4):

Another dissemination channel is to organize public events where the outputs of the project are presented to experts and professionals, and to the general public. The target is to have one or two public events.

Brochures (Task 7.1, Deliverable D7.1, D7.4):

Issue brochures, leaflets, bulletins and handouts describing the project activities and results, as well as dissemination material for end user groups, using both physical and electronic means.

Newsletters (Milestone M7.1):

Distribution of electronic newsletters through the Internet and bulletin boards as well as creation of WWW server open to Internet. The newsletter is intended for the project partners and, importantly, to a more general audience.

Website (Milestone M7.1, M7.6):

A website will be developed in order to provide a continuous update about the project progress and results. There will be information about all the consortium partners, their background and contribution inside NAVOLCHI. All the deliverables and publications will be uploaded on the web site. An updated area will provide all the necessary information about the presence of the project in conferences and exhibitions. The site will be updated regularly, and will be active for at least a year after the end of the project.

Press (Milestone M7.2, M7.7):

Press releases, news-bulleting, press conferences and interviews will be organised for relevant European and national trade newspapers as well as publication of corresponding papers, journals and articles.

B3.2.2. *Exploitation Activities*

The purpose of the corresponding activity is to exploit the knowledge and yield of the NAVOLCHI project by the consortium partners. Exploitation will be performed in terms of extending partner knowledge on a specific area or acquiring knowledge in another, commercializing products that have been developed during the project duration, and/or granting royalty-based access rights to foreground resulting from the project.

Industrial Partners

ST-i ISG (Interconnect Systems Group) is responsible for the development and delivery to ST division and external customers of both on-chip and off-chip communication systems for a variety of applications, such as Set Top Boxes, DVD players and recorders, digital still cameras, automotive, TV, computers, mobile phones and others. Some of these applications require the systems to be split in different chips for reasons linked to technology (digital, analog, and power supply voltage), available space (IPs area, pads) and modularity (design reuse), according to the System in Package (SiP) approach. By participating to NAVOLCHI project ST has the opportunity to develop a state of the art off-chip communication system for SiP applications relying on an extremely innovative physical layer (PHY) based on the disruptive plasmonic technology. The power of the new solution ST will have will be demonstrated by the various benchmarking activities forecasted by the project plan.

Research Centres and Academia

All research centres and the academic partner involved in NAVOLCHI have state-of-the-art experience in the area of photonic components and subsystems and their applications in communication technologies. Research centres and academia will spread project results through lectures presented in academia, industry. In addition they will actively participate in conferences and scientific workshops representing the project and presenting relevant project results. They will try creating spin-off SME companies. Research centres and academia in the consortium possess specialized exploitation centres and have direct connections with industry. In more detail:

KIT: Karlsruhe Institute of Technology will exploit the results of NAVOLCHI in student and doctoral education, by publishing and also by focusing on knowledge transfer to other research projects and activities. KIT will explore the potential use of the proposed silicon organic photonics technology for future applications, and they will initiate research on new materials and processes for applications not concerning optical networking (sensors, medical devices, etc). Partner KIT has just recently founded a spin-off company and will also explore initiations of spin-off companies out of the successful research groups supported by the NAVOLCHI project activity and will take advantage of the new industry contacts. Internal exploitation of the project's R&D work includes publications as well as valuable input to other related activities, while IP generated during the project will be patented where applicable.

IMEC: IMEC (Ghent University) is a European leading research department with more than 300 papers published and many patents filed in the field of the advanced technologies of photonic components and subsystems. IMEC will continue their strong dissemination efforts in renowned journals as well as at major conferences and at websites such as www.optics.org. The involvement of IMEC in the NAVOLCHI project will significantly add to the training of Master and PhD students. The knowledge created in the NAVOLCHI project will add to the quality of the photonics and telecommunication courses at IMEC in general. IMEC will integrate the developed processing capabilities into its silicon photonics platform process and work out standard modules, i. e. processes and standard building blocks. When suitable, these modules can be made available to third parties in a foundry-like model such as the existing ePIXfab initiative. IMEC also has extensive experience in technology transfer to industrial silicon foundries, which can enable larger-volume product if the technology becomes sufficiently mature.

IMEC will take advantage of the intellectual property generated through NAVOLCHI by securing patents for new inventions and by exploitation of know-how in commercial ventures (e.g. licensing and consulting services) or future research projects. IMEC iss well-established IP management policy evaluates relevant results for patentability prior to publication.

UGent: Ghent University will exploit the results of NAVOLCHI in student and doctoral education, by publishing and also by focusing on knowledge transfer to other research projects and activities. Within NAVOLCHI, UGent will develop and characterize novel colloidal quantum dots emitting in the near IR for applications in Si photonics. These materials are relevant to the whole of the expanding research activities of UGent in the field of nano- and biophotonics within the multidisciplinary research center NB-Photonics. In practice, the know-how developed within NAVOLCHI is transferable to research fields including solar concentrators for photovoltaics, luminescent probes for bio-imaging or light sources in the Mid-IR. In this way, the NAVOLCHI R&D work will lead to additional publications and will provide input to related research activities. In addition, IP generated during the project will be patented where applicable.

TUE: Eindhoven University of Technology will exploit the results of NAVOLCHI in student and doctoral education, and also by publishing and employing the results in other research projects. TUE is expanding its program on plasmonic nano-lasers and the ability to make nano-lasers on SOI wafers will be a great bonus to this program. In particular there is already a program at TUE looking at implementing active InP structures on SOI using a membrane waveguide structure. This inclusion of plasmonics into the SOI membrane concept will complement this other program. In the future it is the view of the optoelectronics group at TUE that eventually most integrated optics circuits will migrate to such SOI membrane structures. Furthermore, that in the long term plasmonics and plasmonic lasers will become a significant part of integrated optics.

AIT: AIT has been founded as a centre of excellence for research and education in the fields of information technology and telecommunications with the vision to serve as a bridge between academia and industry in Greece. A number of over 70 postgraduate students are enrolled in the three graduate programs of AIT. Moreover, AIT offers market-targeted professional courses to industry on several topics related to IT and telecoms, including next generation networks and access-metro-core technologies. Finally, AIT has already connections and well-established collaborations with local telecommunication operators and system vendors in the form of non-disclosure agreements (NDA). AIT plans to use the results obtained within the project in order to: a) further enhance its knowledge and competence in the field of optical telecommunication networks, b) spread this knowledge through educational and industry oriented courses and preparation of specialized teaching

material and c) improve further its industrial collaborations. In addition to these and according to its chart, it is AIT's intention to build up through participation in NAVOLCHI and other European projects a substantial know-how and IPR portfolio, which can result in foundation of start-up companies.

UVEG: The UVEG group has been recognized as a group of research excellence in our region and will pay special attention to publish results in high impact journals and exploit results of NAVOLCHI at Master and PhD education levels. The group has a strong expertise in physics and optical properties of semiconductor nanostructures and have been setting up in the last three years a new chemistry lab dedicated to the chemical synthesis of metal (Ag, Au) and semiconductor nanoparticles (CdS, CdSe, CdTe and PbSe, at the moment, covering light emission from 400 nm up to more than 1700 nm). At the same time, polymer based nanocomposites were also developed in this lab as the basis for UV and Ebeam patternable resists loaded with such nanoparticles. Several important papers have been published in the case of metal nanoparticles synthesized in the same polymer during Ebeam exposition or using a post bake after UV photolithography (this technology was patented in 2008). Part of this know-how has been transferred to Intenanomat SL (recently recognized as spin-off company at the University of Valencia), but the company will actively participate with the UVEG group in collaboration with a new Chemistry posdoc researcher (to be hired in next months within the European Strep Project NANOPV, and continue within the scheme of this project). Intenamat is very interested to collaborate in developing hybrid materials (patternable polymer/metal and polymer/metal/semiconductor), because it could be the basis for the future introduction in the market of special inks (or pastes for spin-coating) to develop applications in organic photonics and optoelectronics, like the ones proposed in NAVOLCHI. Therefore the spin-off company of the UVEG group will be involved in exploitation activities that could be suggested by NAVOLCHI during its development

B3.2.3. *Management of knowledge and intellectual property*

Matters related to management of knowledge and intellectual property handling will be defined in the "Consortium Agreement," where rules will be defined to identify and protect the result of the NAVOLCHI work, especially innovations. The Consortium Agreement will be aligned and follow Commission policy on knowledge and intellectual property and will tackle:

Ownership and protection of foreground: Foreground will be the property of the consortium member that has generated it. If more than one member has contributed to the generation of foreground, foreground will be owned by all contributing members. Foreground protection will be pursued through patents by foreground owners, under consensus of all consortium members.

Confidentiality: Any material of a confidential nature supplied to the project will remain strictly for the information of project participants and such information will not be forwarded to any other parties without explicit authorization from the information proprietor.

Publication of foreground: Foreground will be published only by its proprietors (either during the project or after the project duration) and under no circumstances a consortium member will publish the foreground of another member.

Access rights to foreground: Consortium members will grant on a royalty free basis access rights regarding foreground that is required to achieve the project objectives. The terms of access rights for

use (exploitation and further research) will be agreed before signing the contract. Access rights for use will be granted either under fair and reasonable conditions or royalty-free.

Access rights to background: Consortium members will grant other members access rights on background that is required to achieve the project objectives in a manner that will be agreed before signing the contract. Members will include in the Consortium Agreement background that will be excluded from access rights, or granted on special conditions. The terms of access rights for use (exploitation and further research) will be agreed before signing the contract. Access rights for use will be granted either under fair and reasonable conditions or royalty-free.

B4. GENDER ASPECTS

Regarding gender-specific issues no such issues are associated with the objectives and the work that is planned to be performed as part of this project. However, the consortium is aiming to organize a work shop for the young female scientists to focus their attention on new disruptive technologies such as plasmonic and nano-technology. Female scientists with achievements in the field of photonics and plasmonics will be invited from the Europe and overseas. The workshop will be aimed to increase the motivation and co-finance of the female students and employees via the invited presentations and intensive scientific discussions.

APPENDIX - ARELEVANT PUBLICATIONS BY PARTNERS

Recent relevant papers of the partners within the consortium:

KIT – Karlsruhe Institue of Technology

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[2] D. Taillaert, F. Van Laere, M. Ayre, W. Bogaerts, D. Van Thourhout, P. Bienstman, and R. Baets, "Grating couplers for coupling between optical fibers and nanophotonic waveguides," *Japanese Journal of Applied Physics*, vol. 45, no. 8A, pp. 6071–6077, 2006

[3] L. Liu, R. Kumar, K. Huybrechts, T. Spuesens, G. Roelkens, E.-J. Geluk, T. de Vries, P. Regreny, D. Van Thourhout, R. Baets, and G. Morthier, "An ultra-small, low-power, all-optical flip-flop memory on a silicon chip," *Nature Photonics*, vol. 4, no. 3, pp. 182–187, Mar. 2010

[4] D. Van Thourhout and J. Roels, "Optomechanical device actuation through the optical gradient force," *Nature Photonics*, vol. 4, no. 4, pp. 211–217, Apr. 2010.

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TUE – Eindhoven University of Technology

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UVEG - Universidad de Valencia

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